A Tamper and Leakage Resilient von Neumann Architecture

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Aarhus University

joint work with

Sebastian Faust (EPFL), Jesper Buus Nielsen (Aarhus),
Daniele Venturi (La Sapienza, Rome)

Physical Attack on implementations

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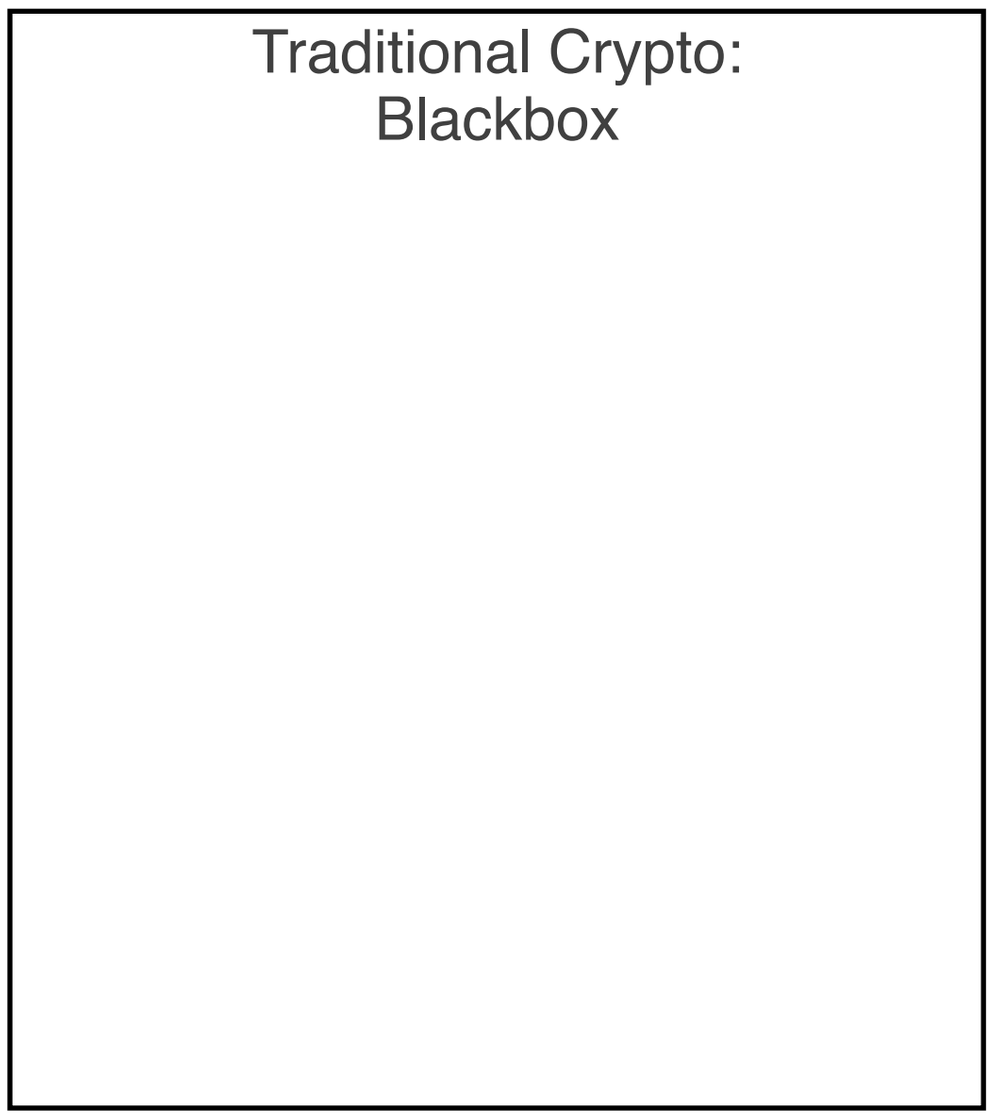

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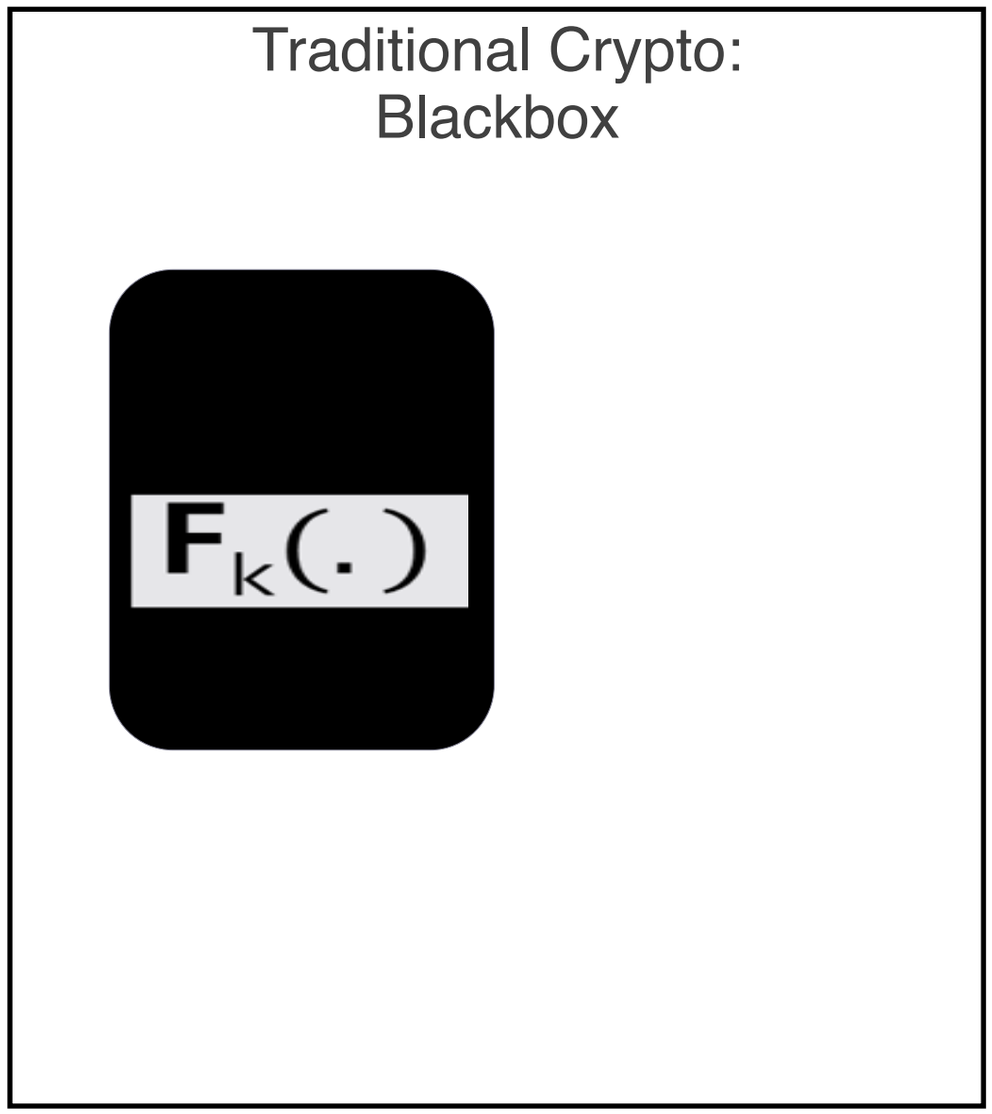

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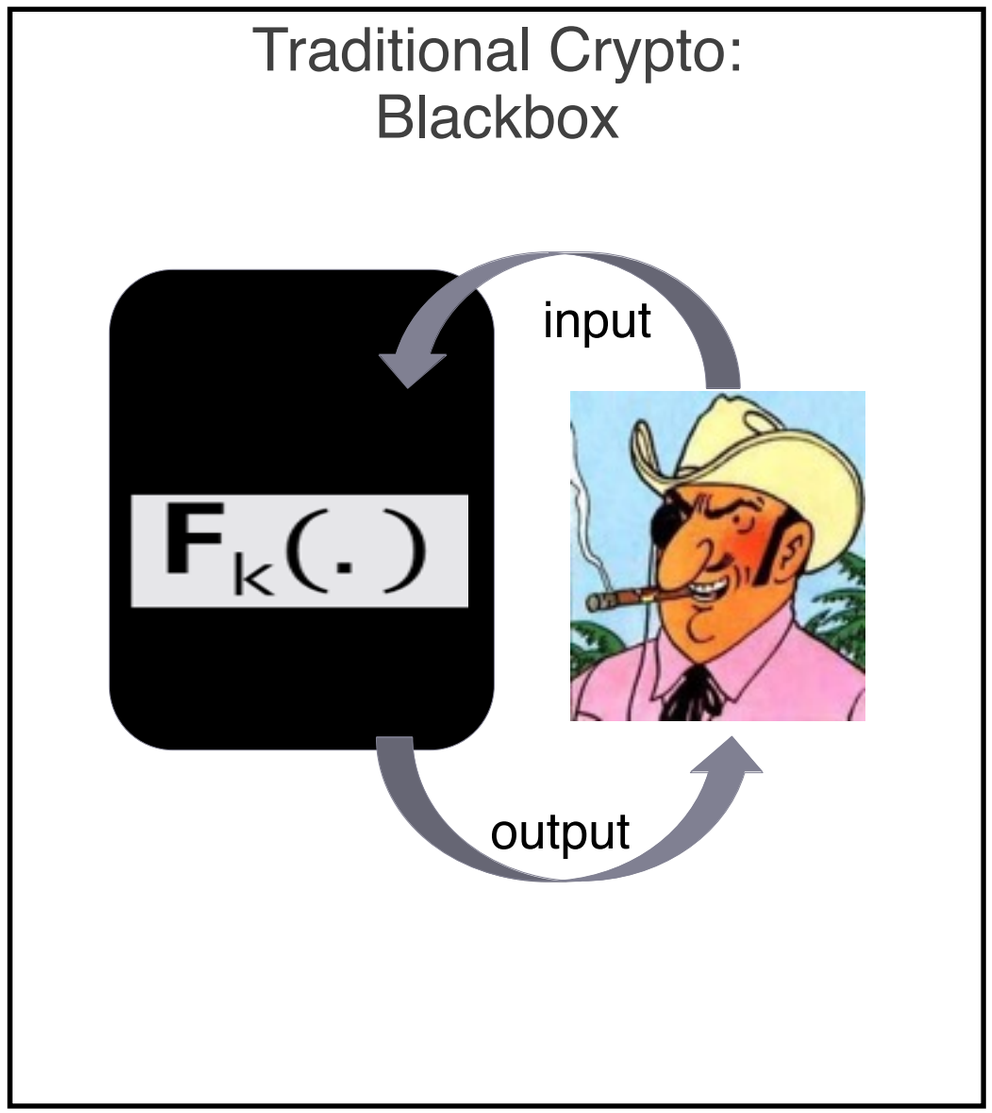

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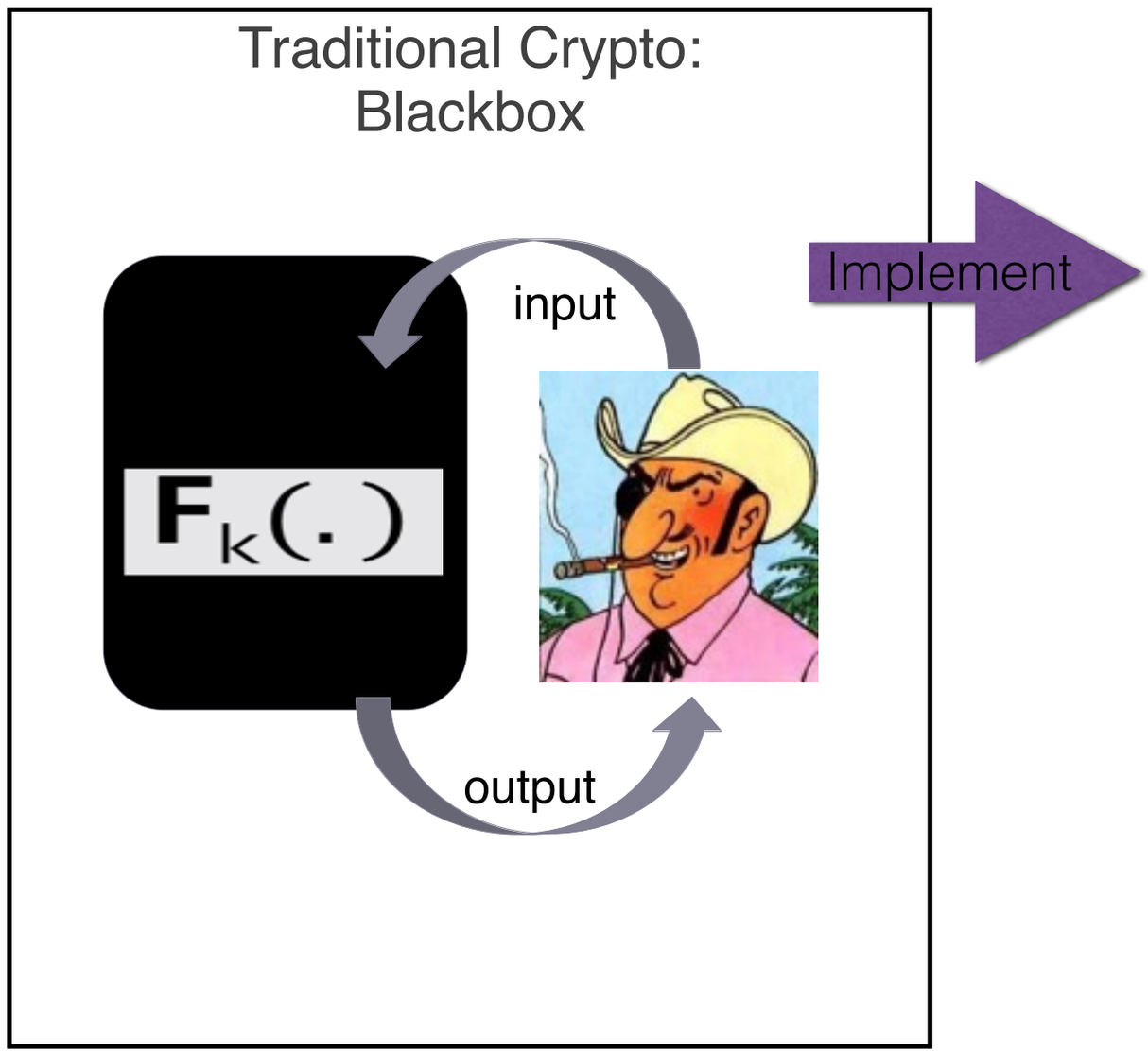

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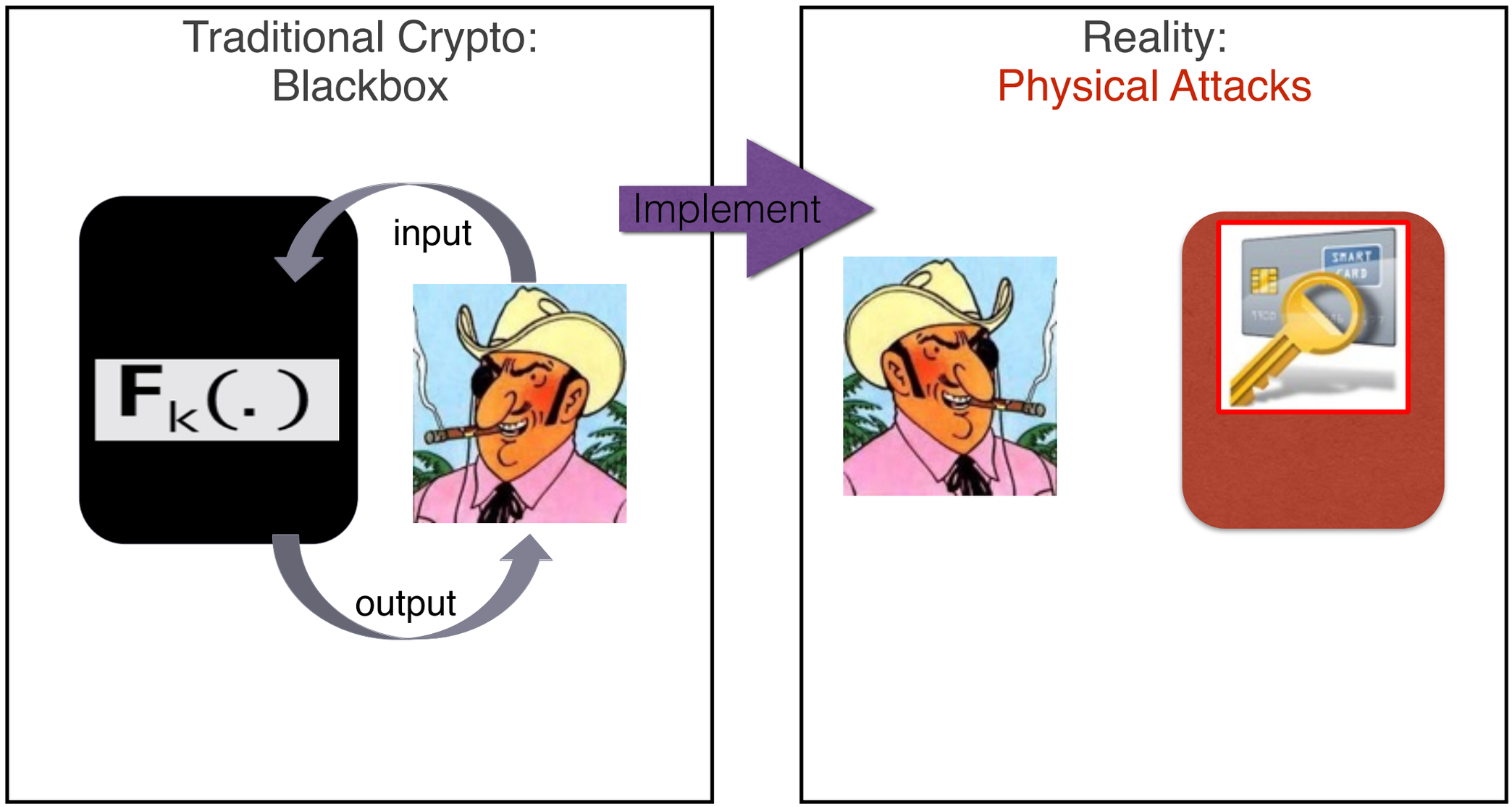

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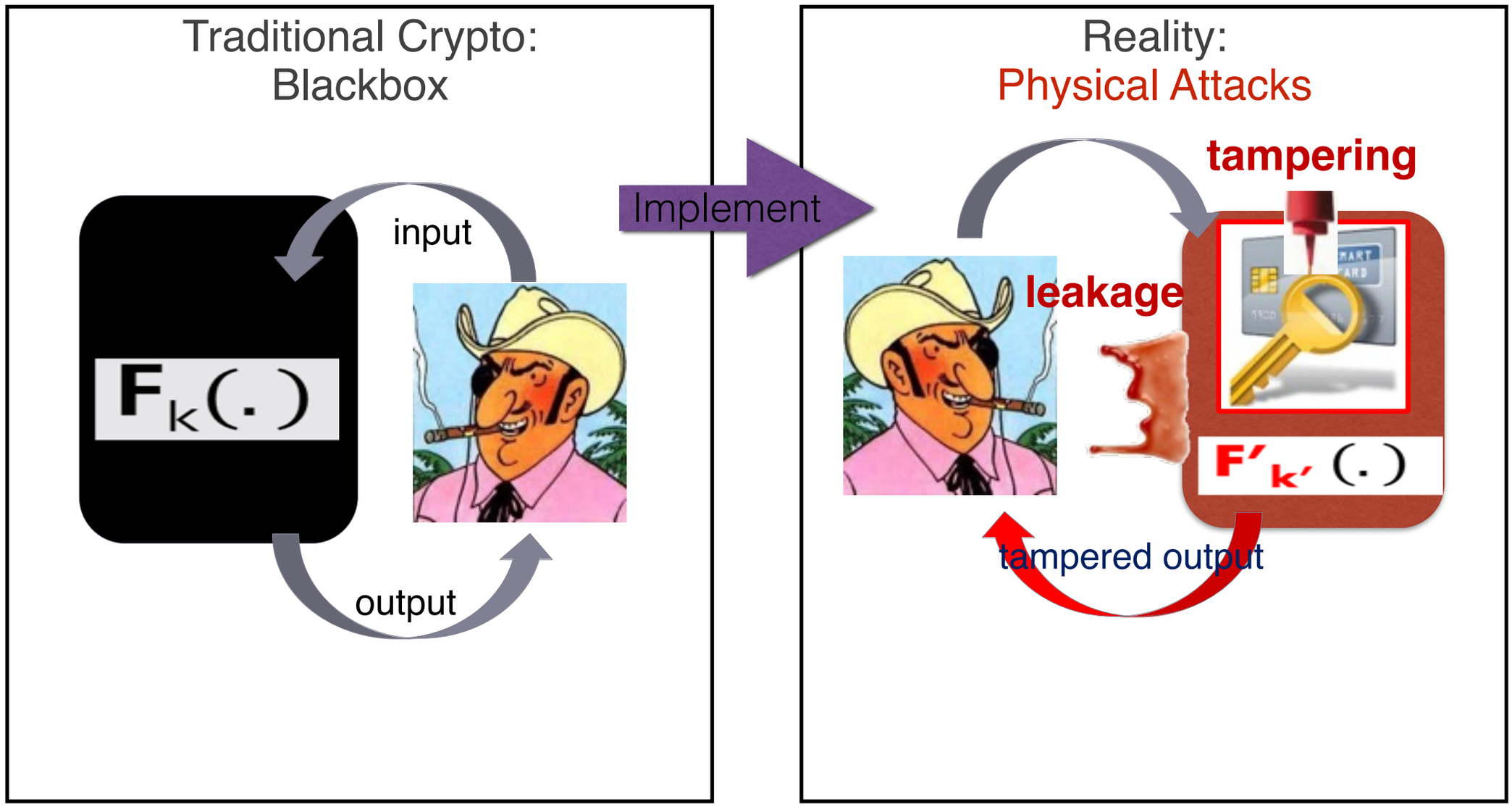

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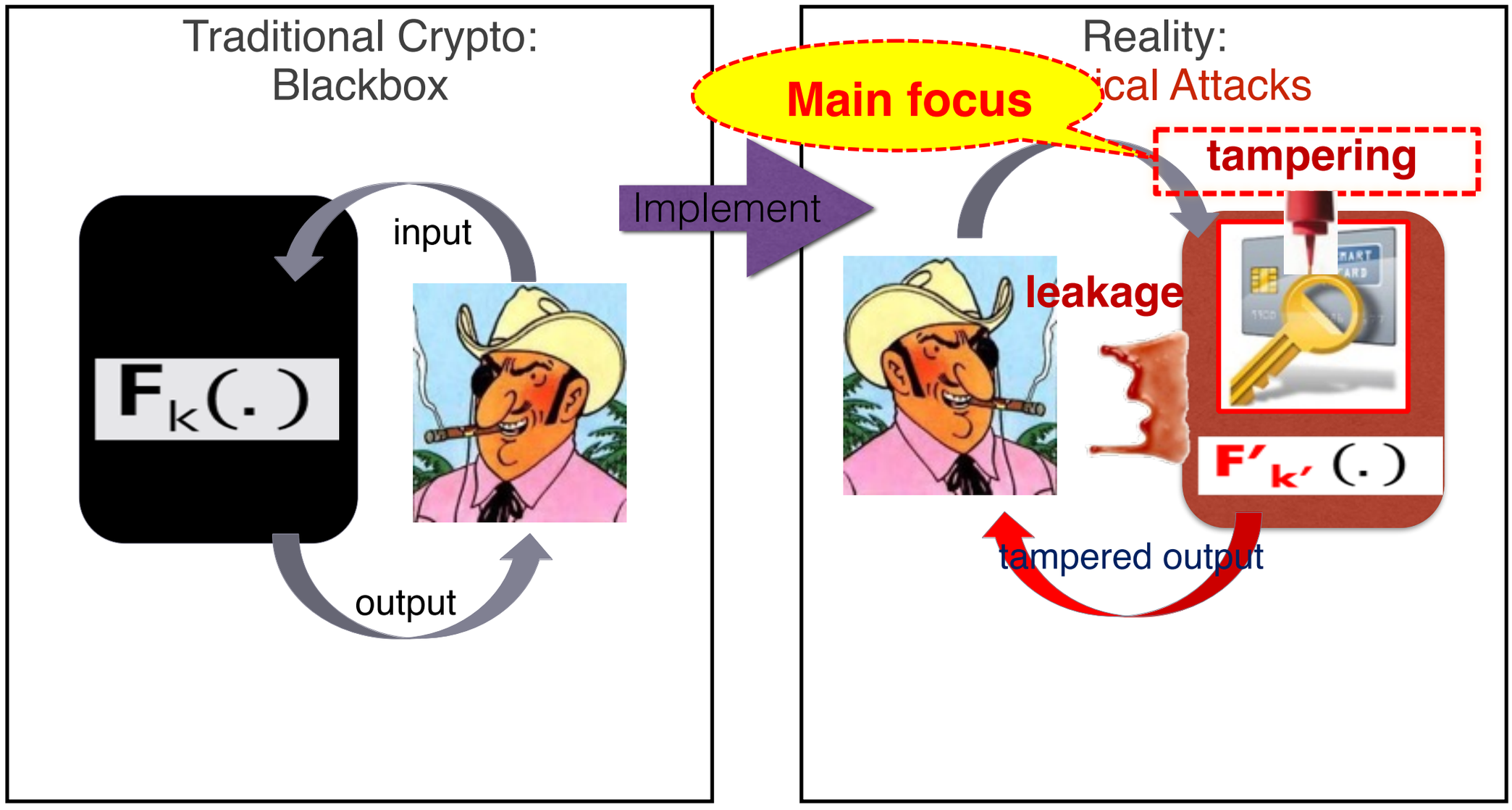

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Factor RSA-modulus !

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Skorobogatov et al. '02

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Devastating attacks on Provably Secure Crypto-systems!

Theoretical Models of Tampering

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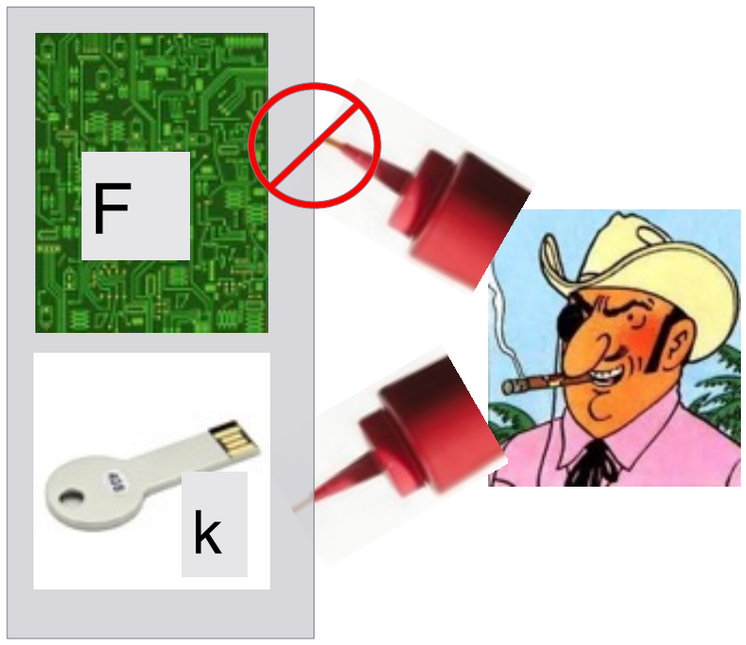
Memory only tampering
(GLMMR ’04)



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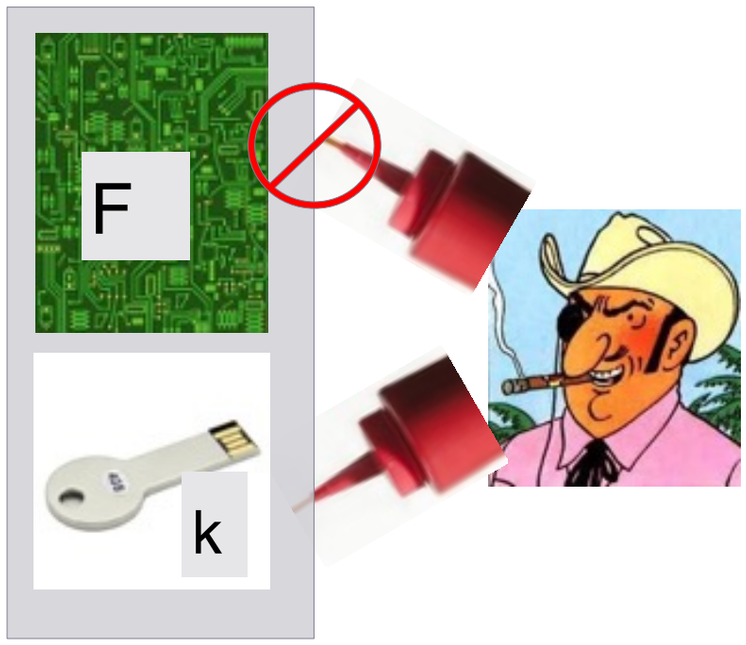

Tamper with both memory and computation
(IPSW ’06)

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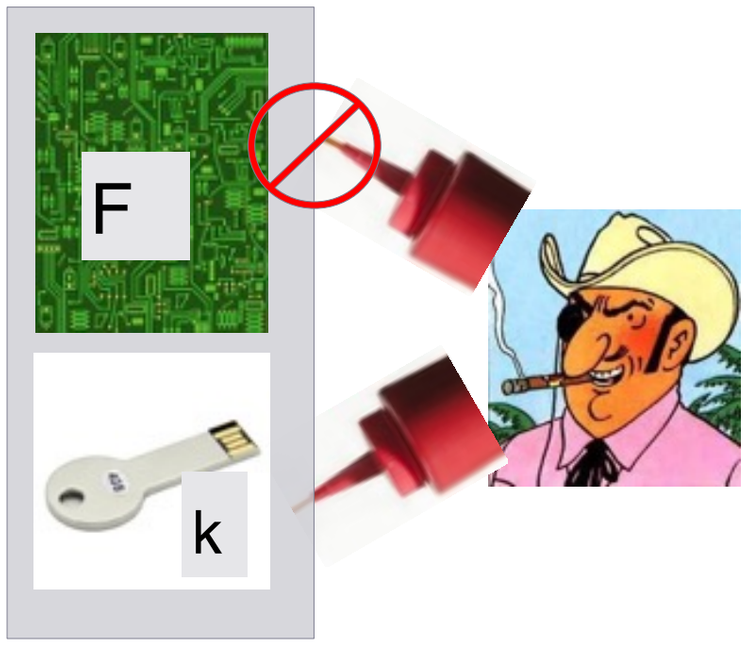

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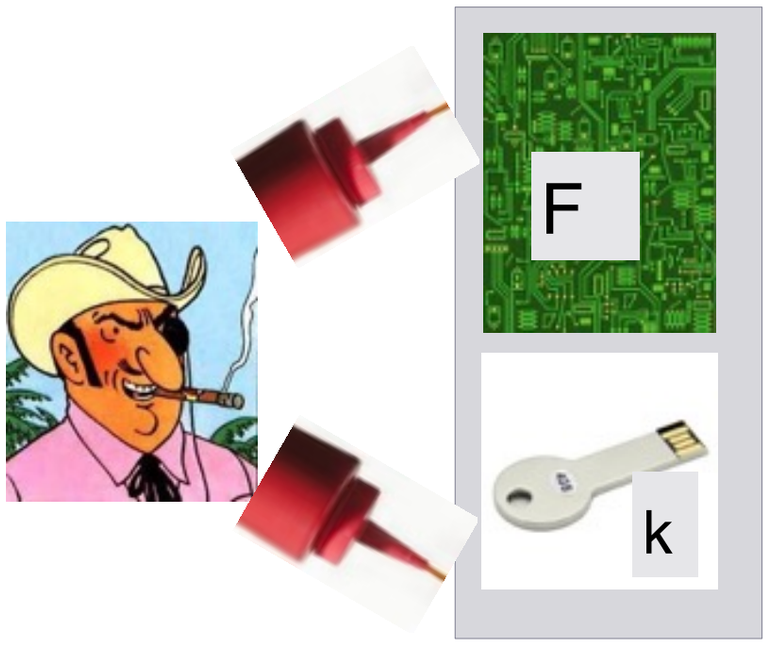

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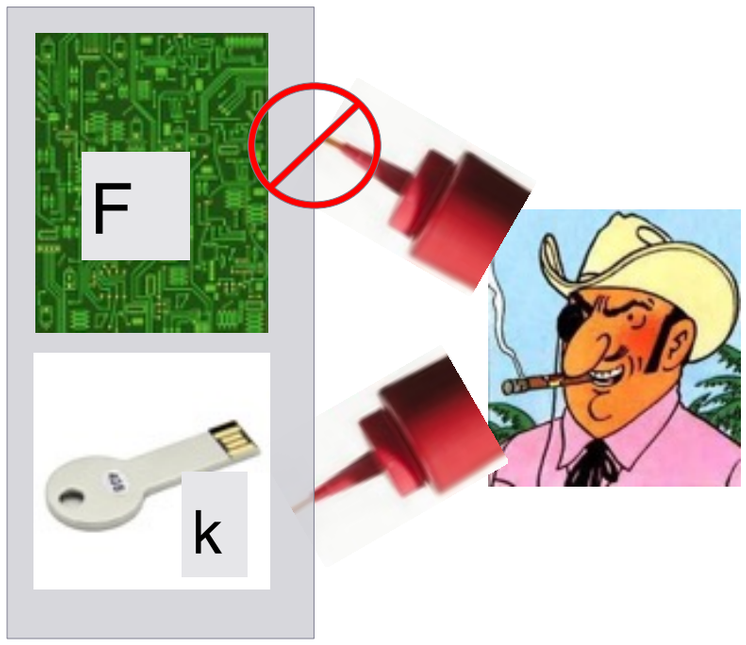

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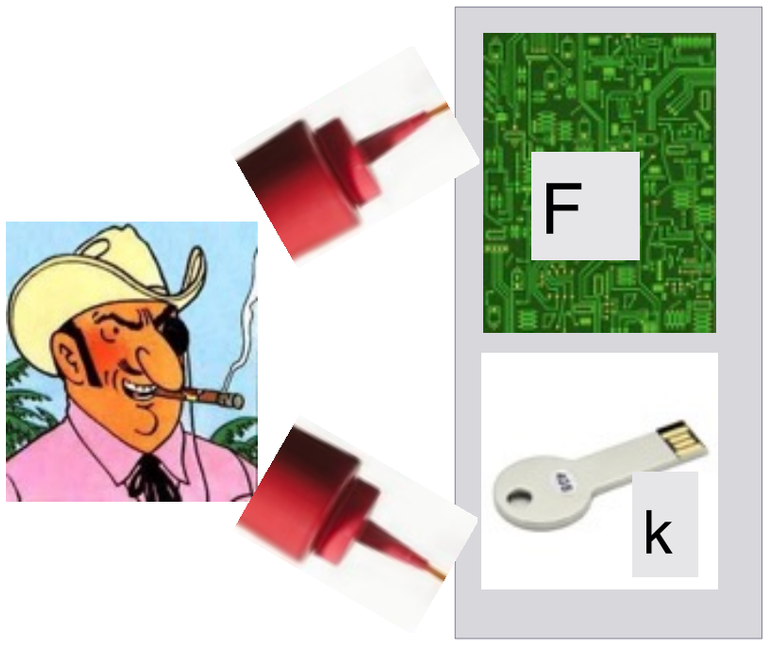

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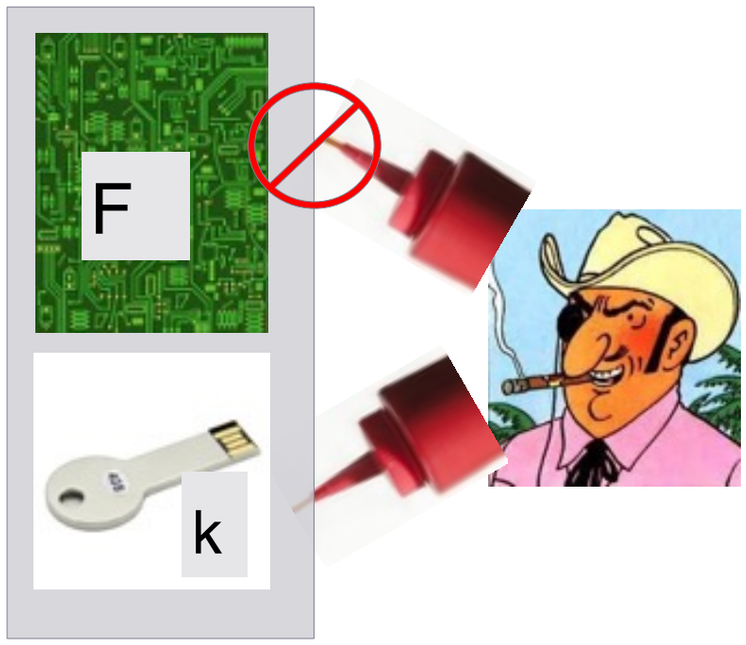

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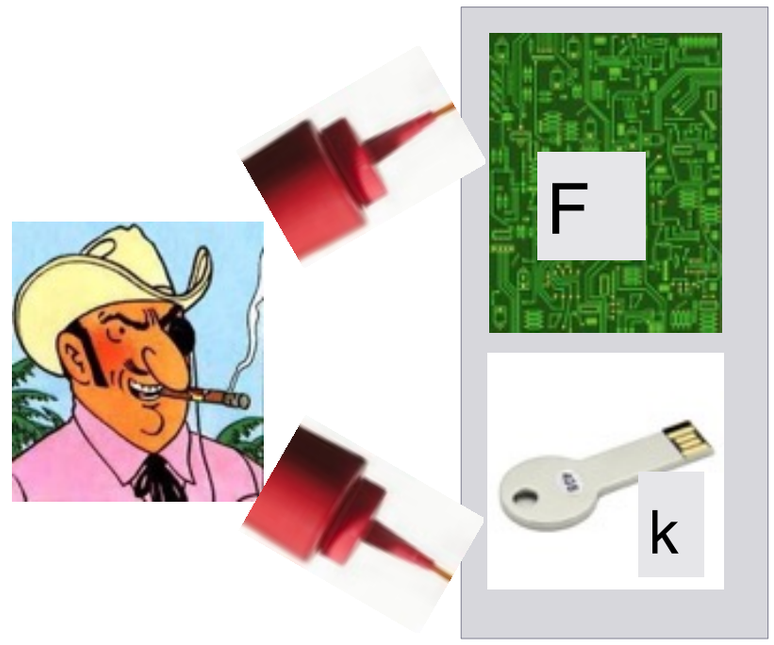

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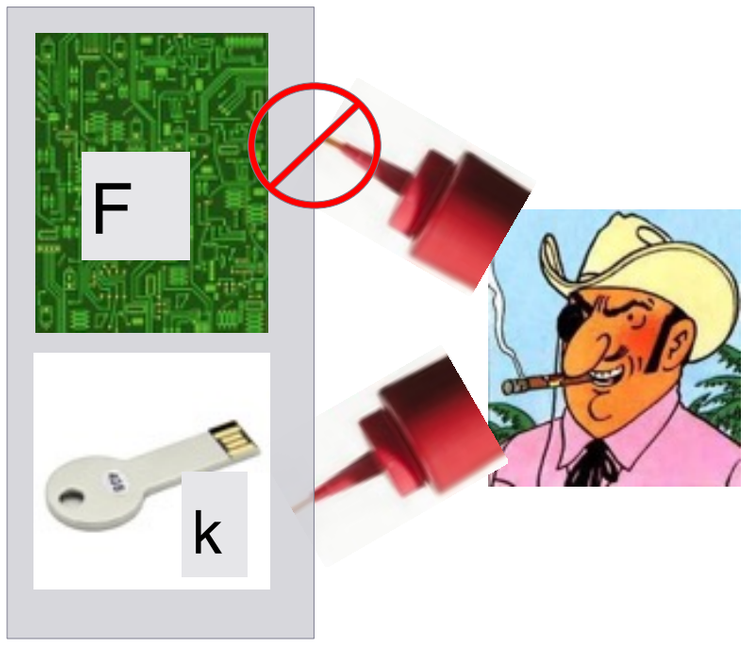

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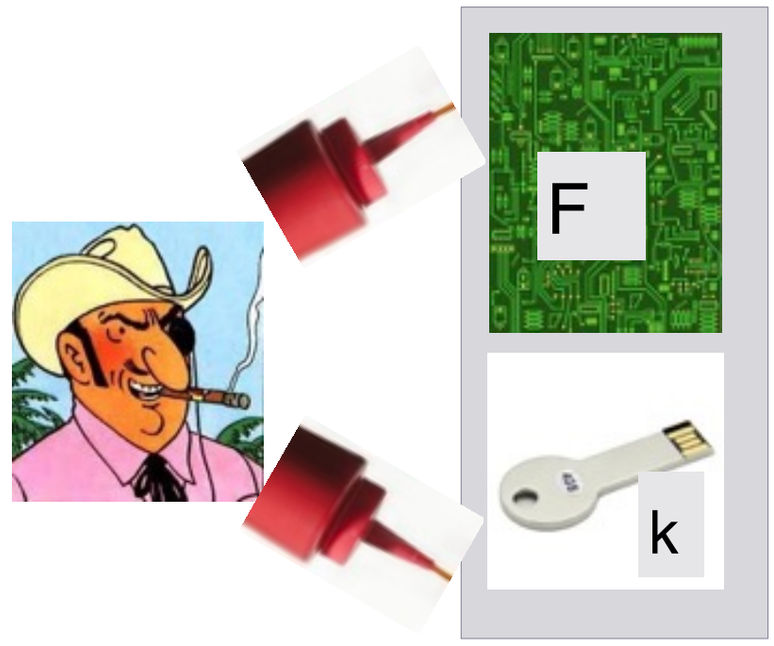

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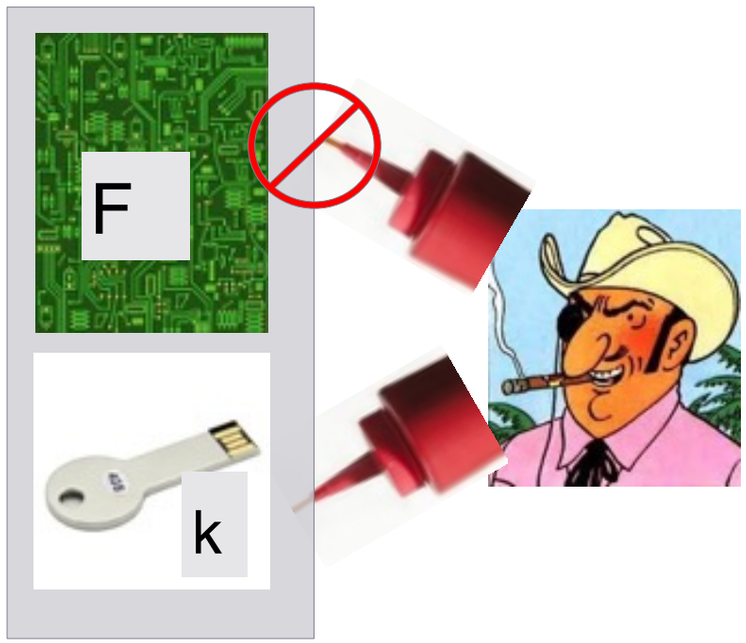

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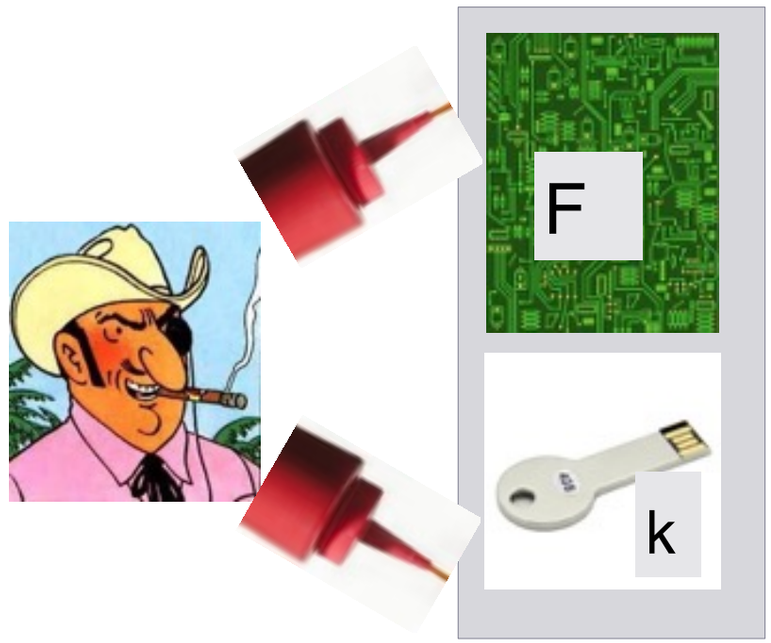

This talk

Earlier approach: protect circuits against tampering

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Current best: DK14:

- Protects against tampering of (1/poly)-fraction of all wires.
- Analysis complicated: involves tools like PCP.

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Current best: DK14:

- Protects against tampering of (1/poly)-fraction of all wires.
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Our goal:

- simpler framework
- stronger tampering adversary

Our approach

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An alternative model of computation:
von Neumann Architecture (vNA)/ Random Access Machine (RAM)

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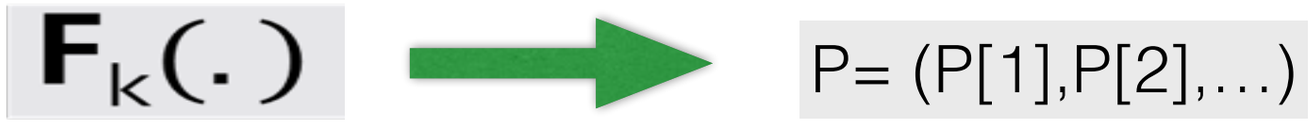

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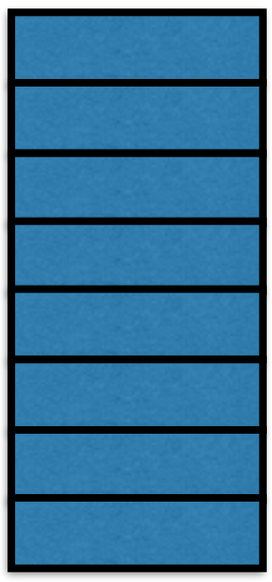
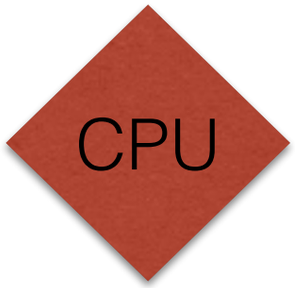
$F_k(.)$ → P= (P[1],P[2],…)



Disk



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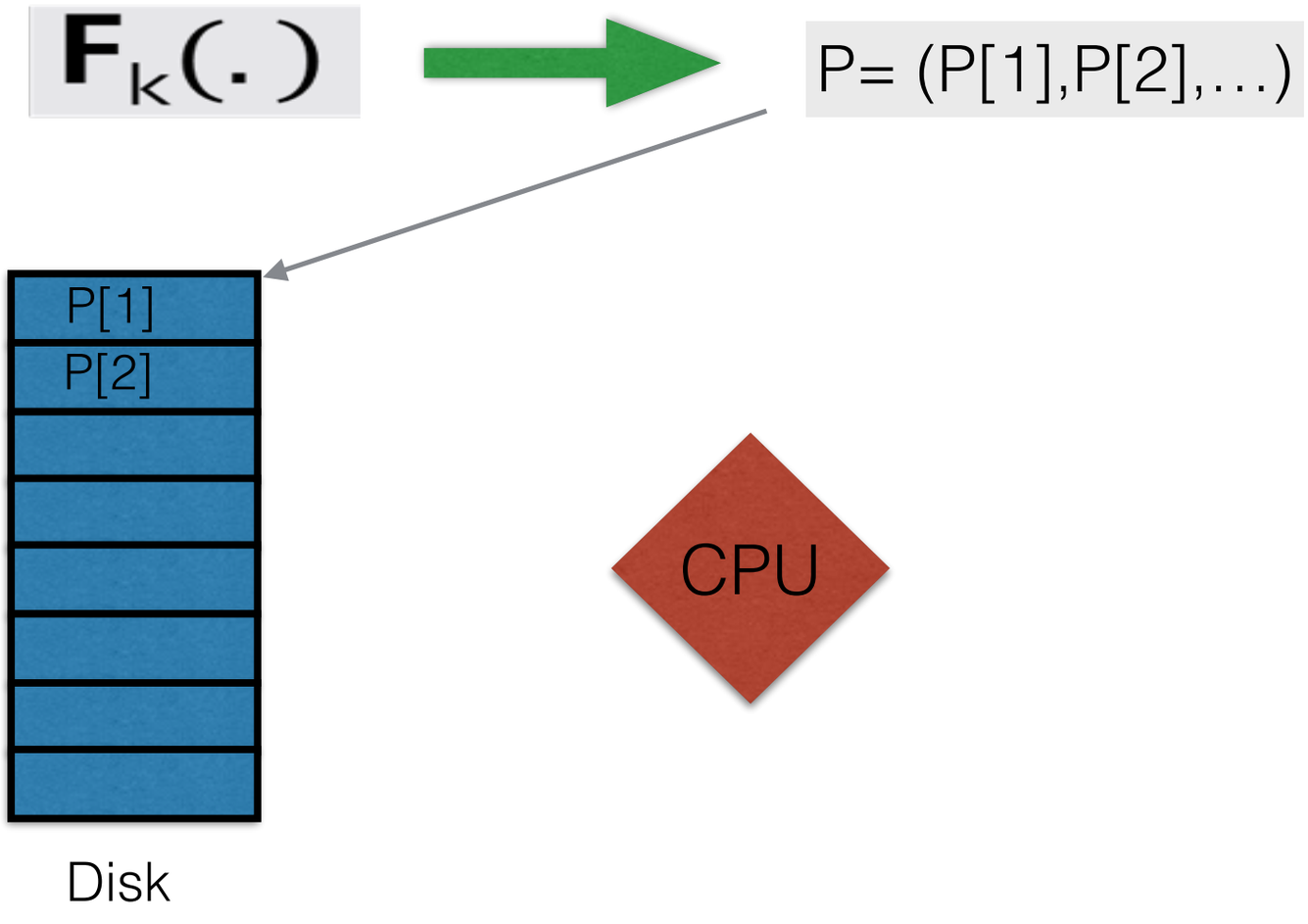

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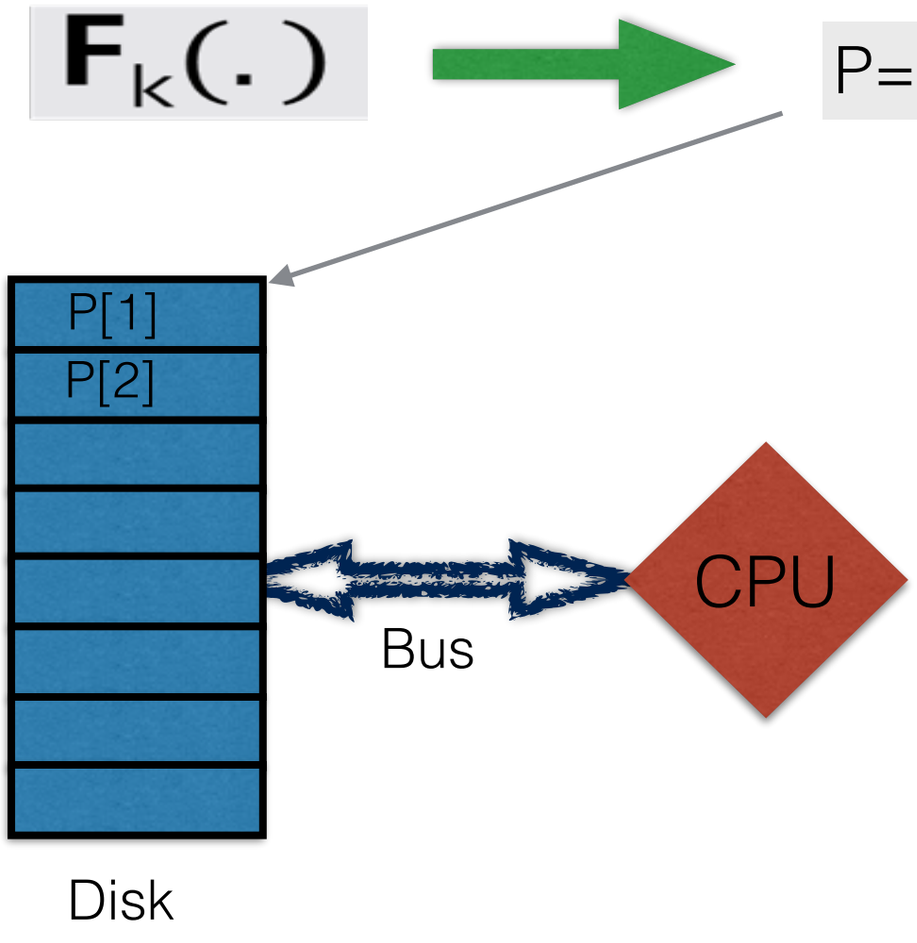

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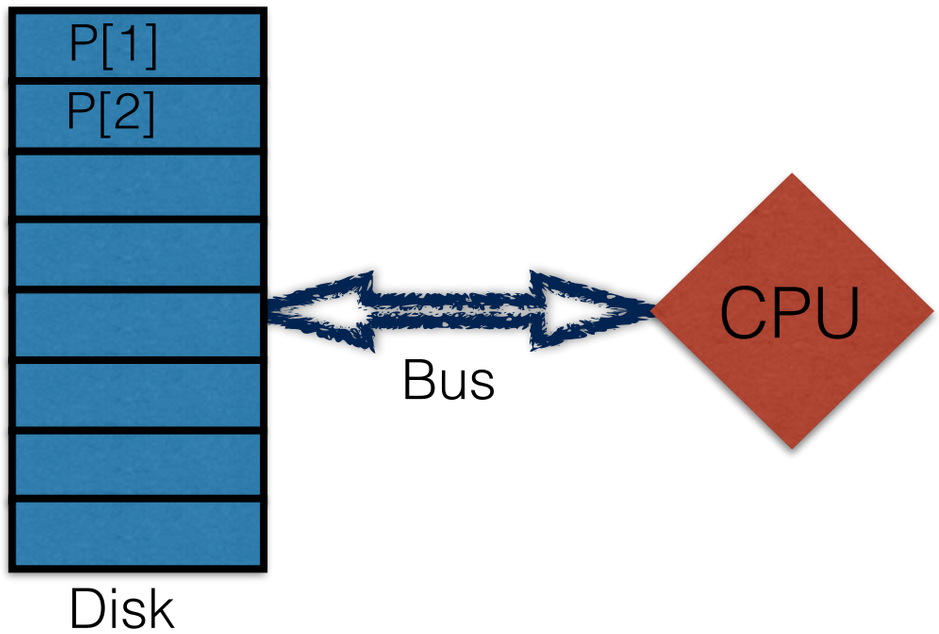

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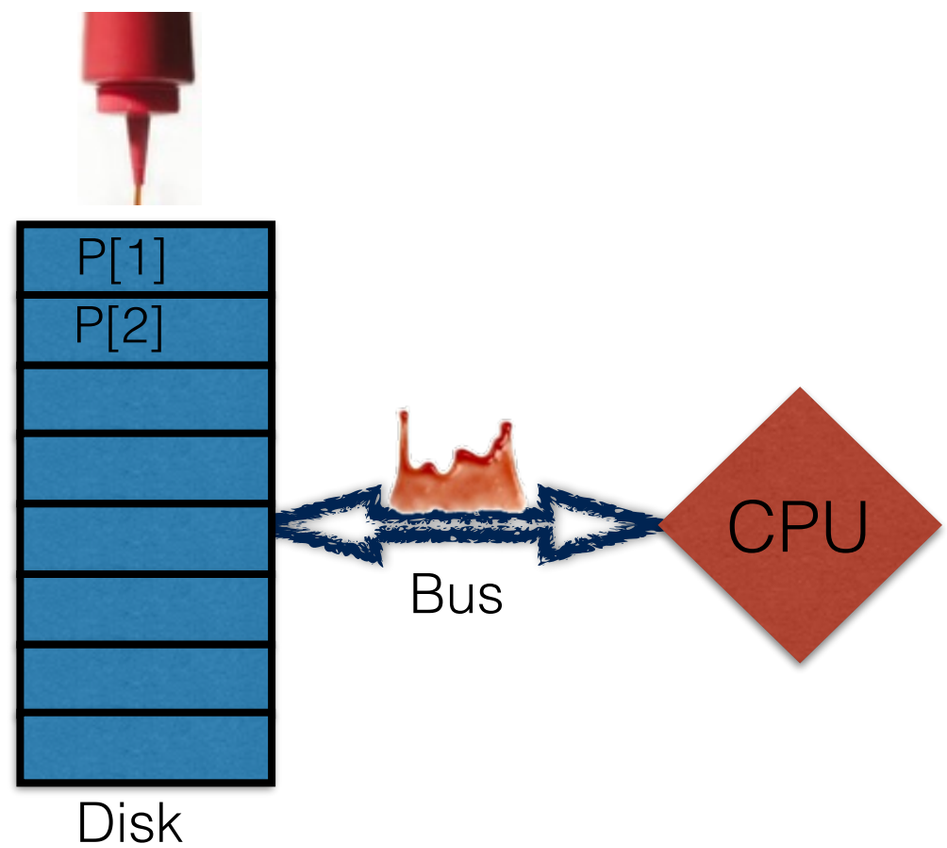

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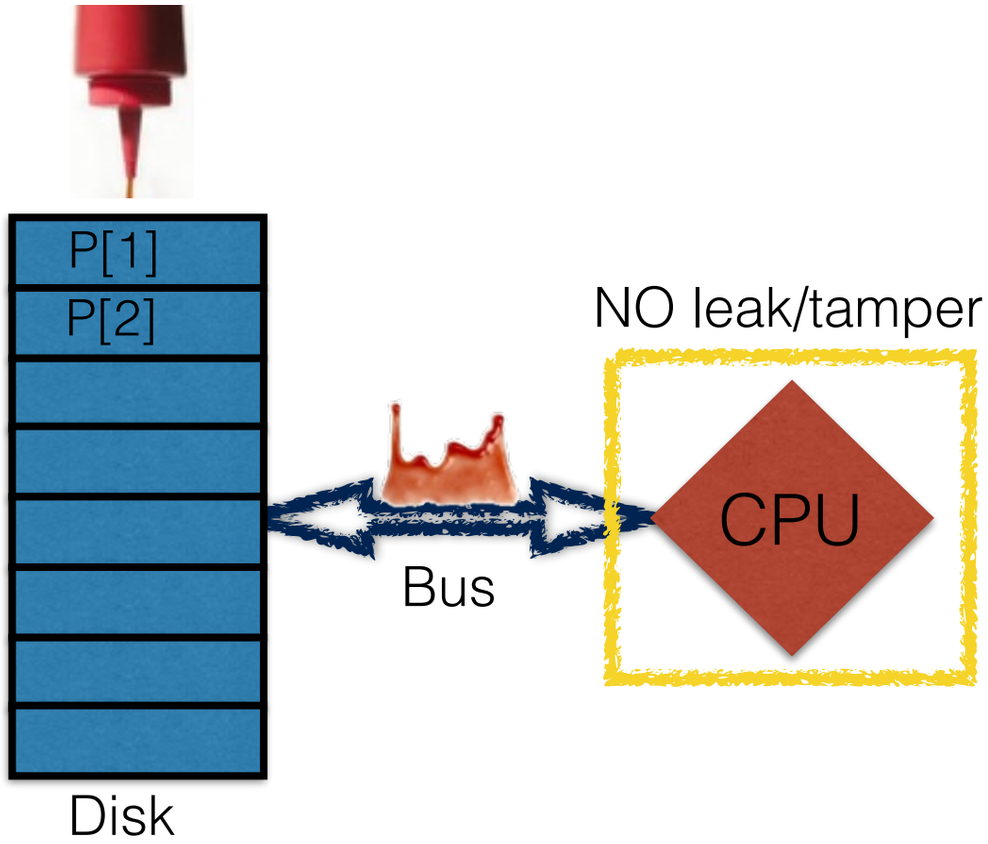

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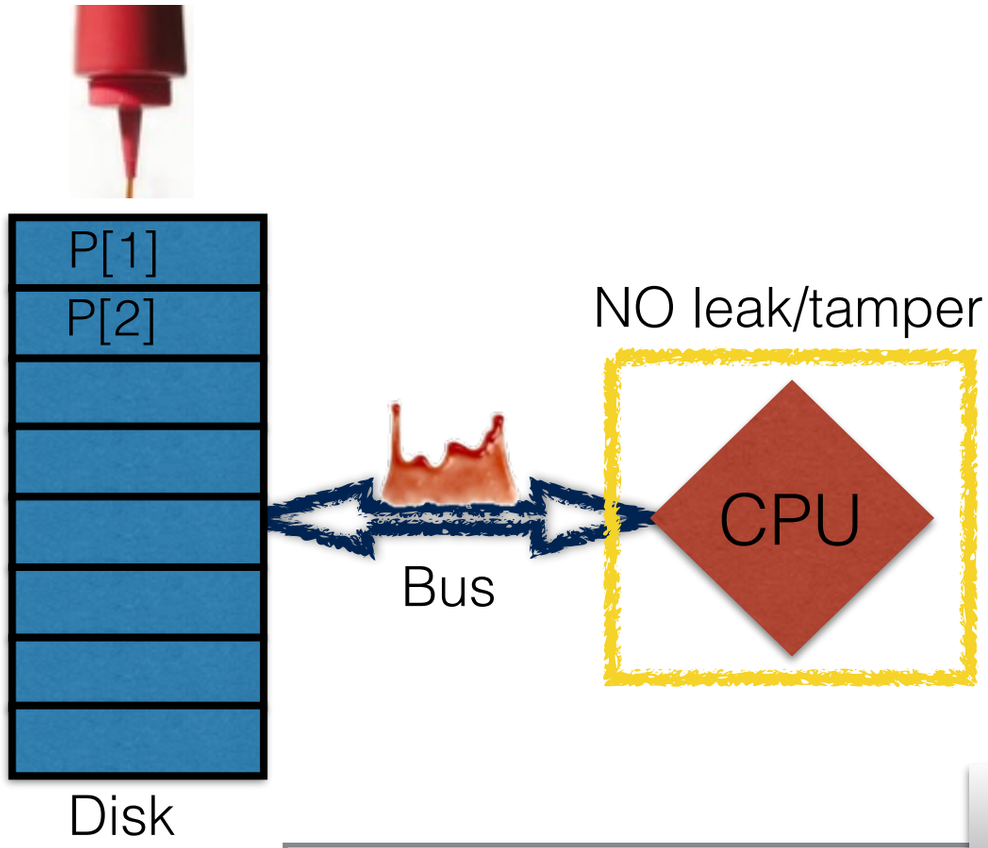
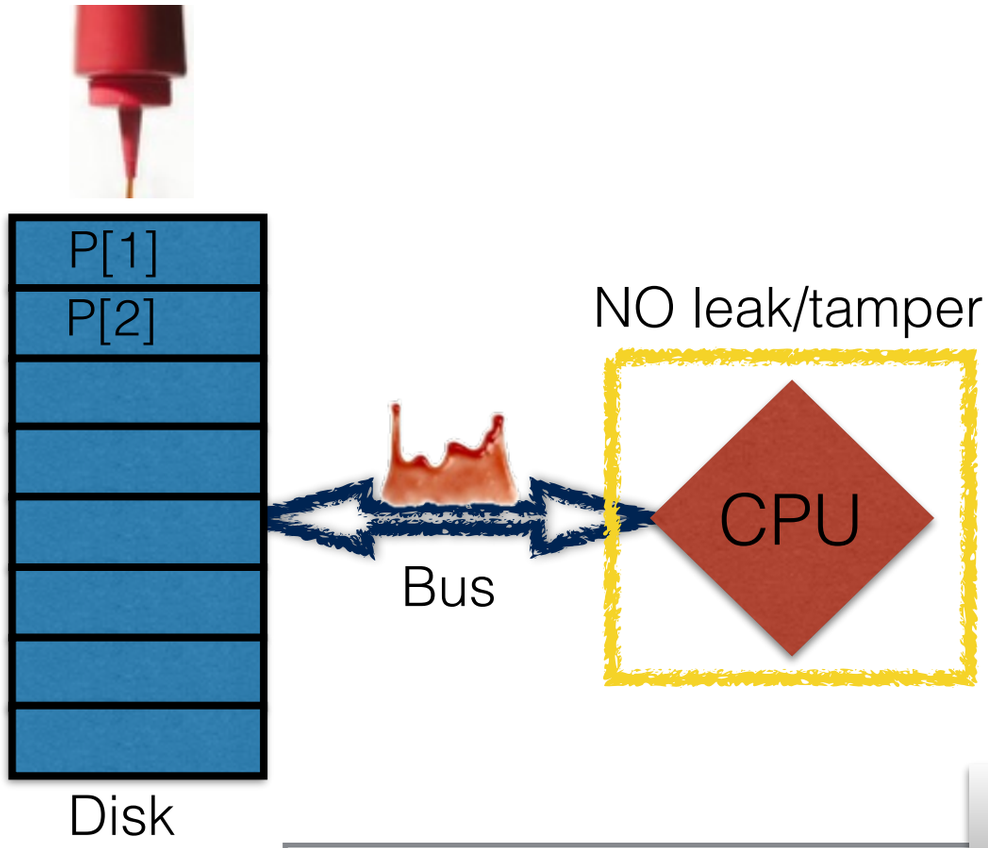


NO leak/tamper

CPU

- “small” and “universal”

Tamper and leakage resilient vNA



CPU

- “small” and “universal”
- Does not store any secret.
  - otherwise simple solution !
  - stores a untamperable special purpose bit.

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DLSZ15: A concurrent and independent work

Locally Decodable and Updatable Non-Malleable Codes and Their Applications

The security notion

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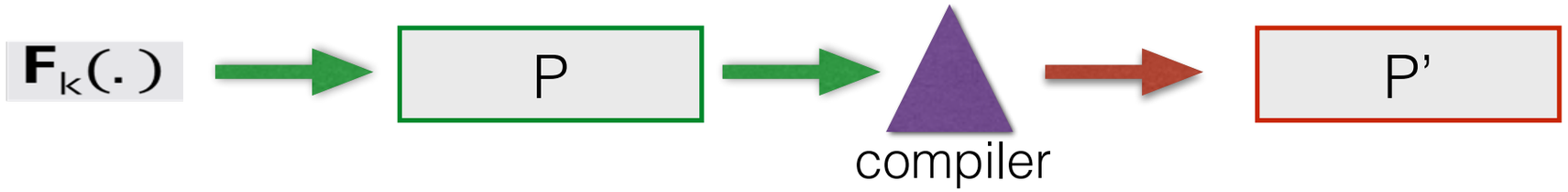

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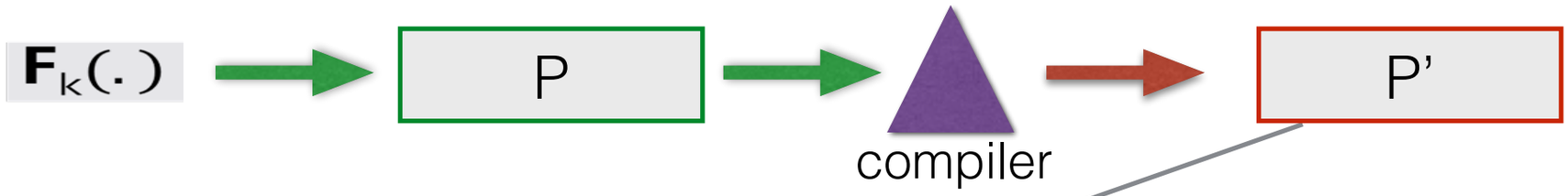

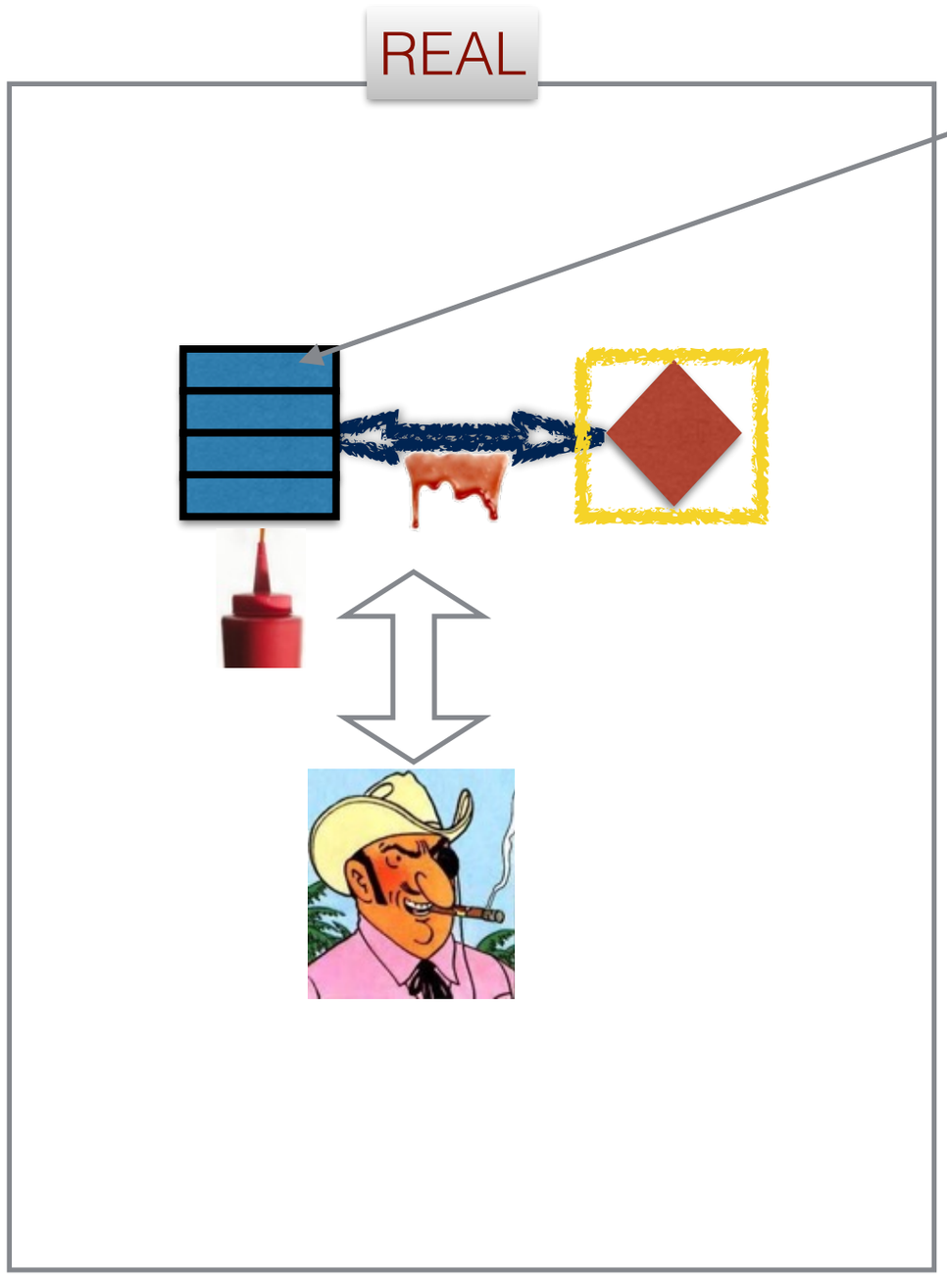

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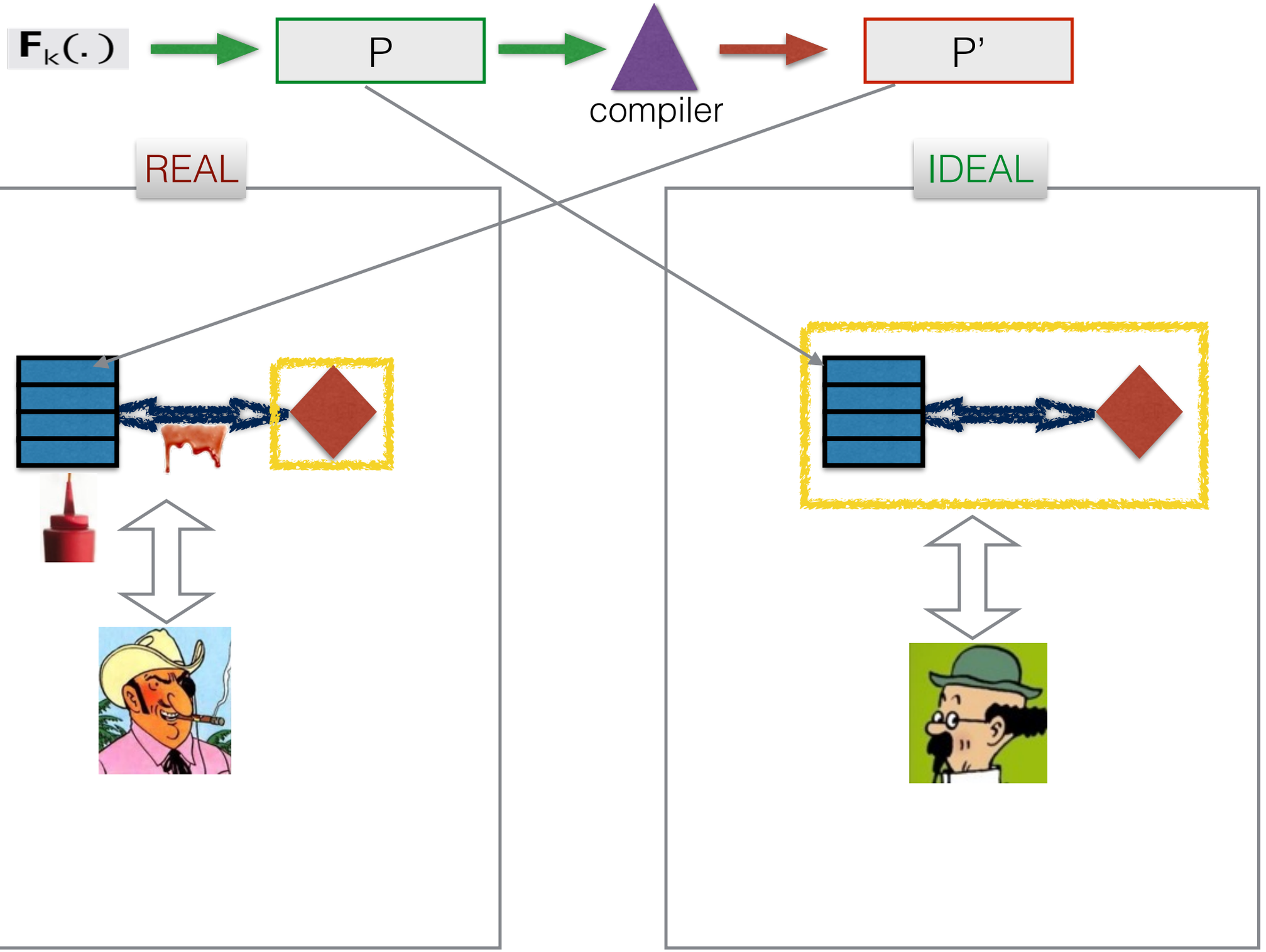

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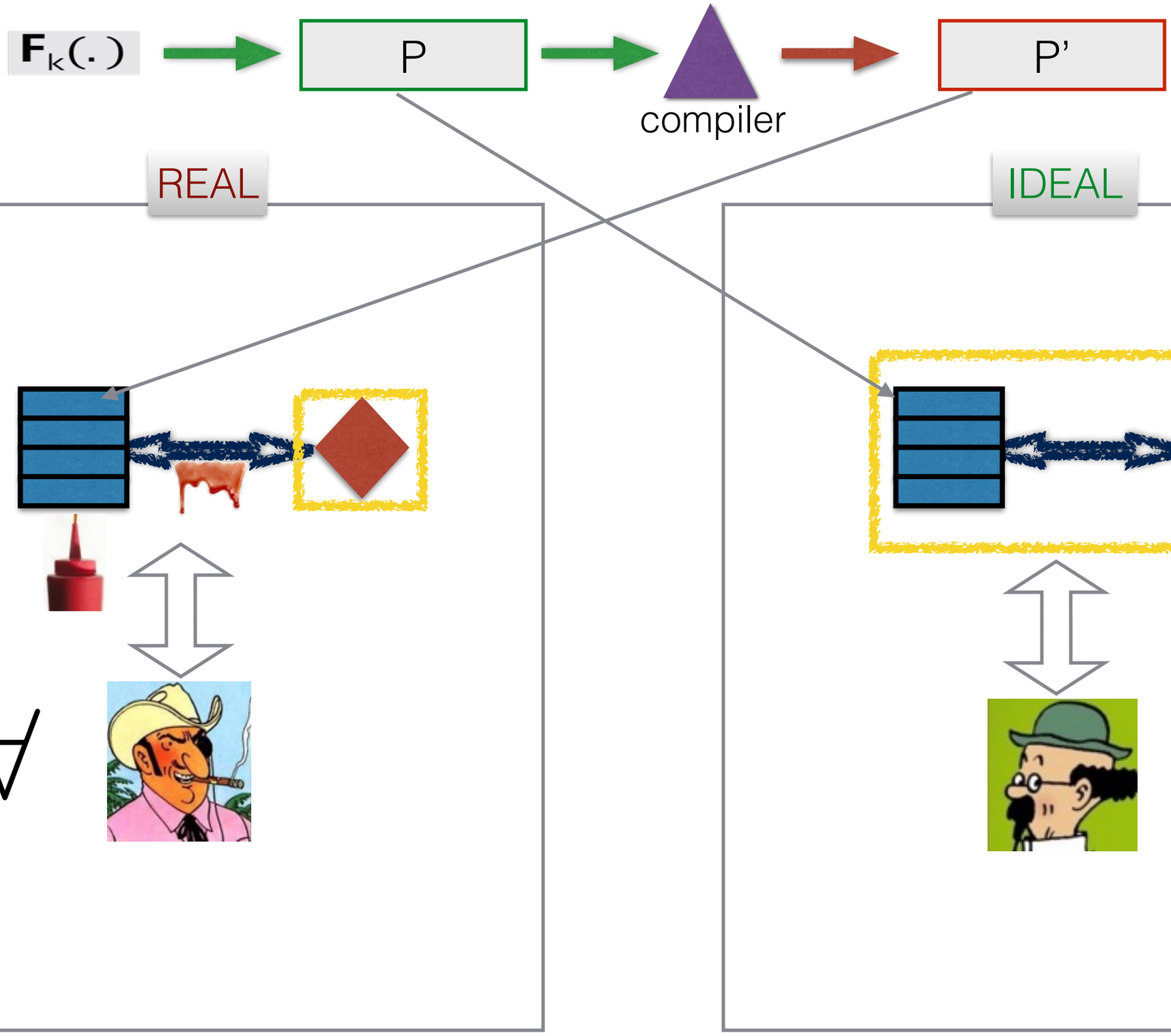

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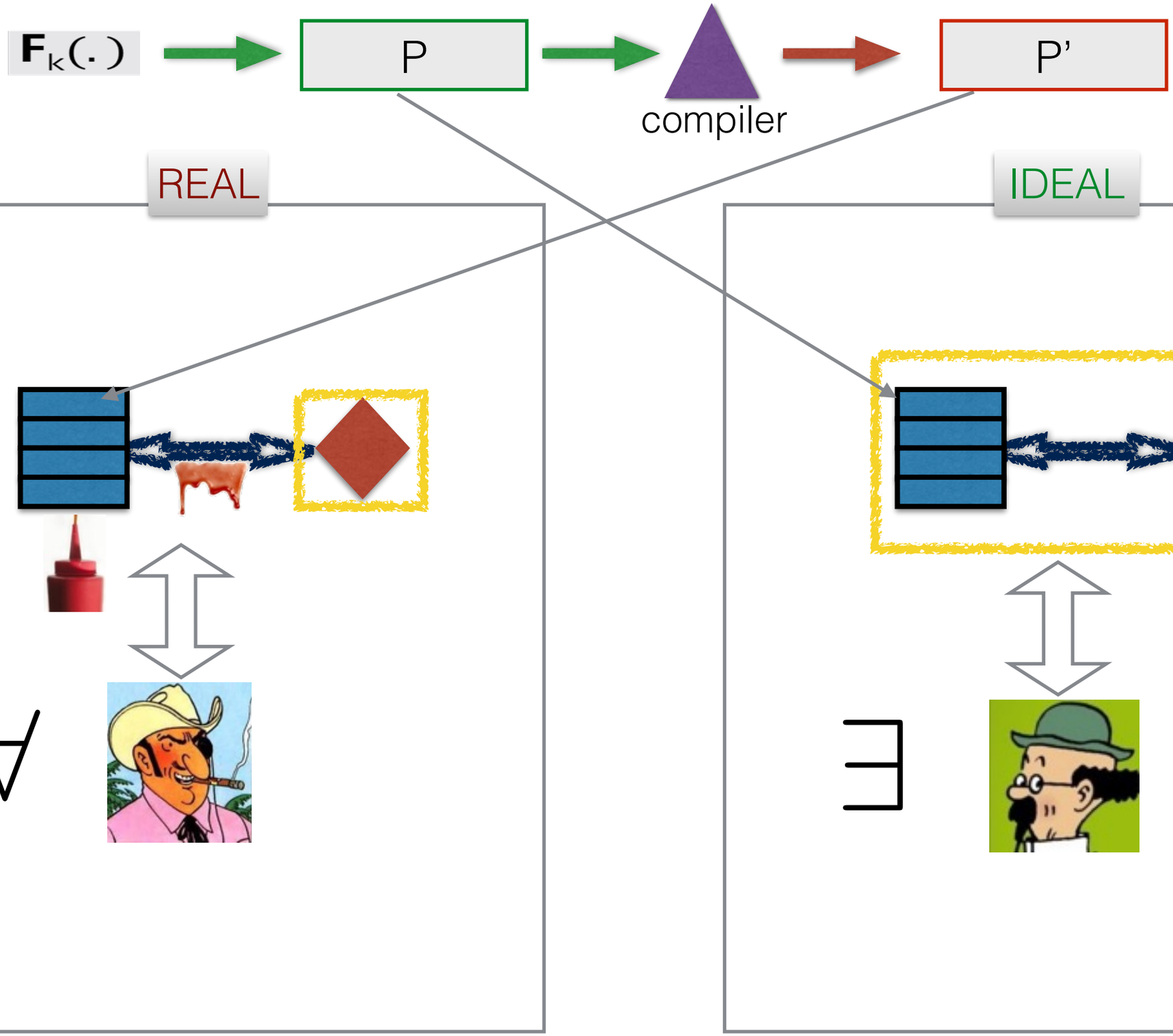

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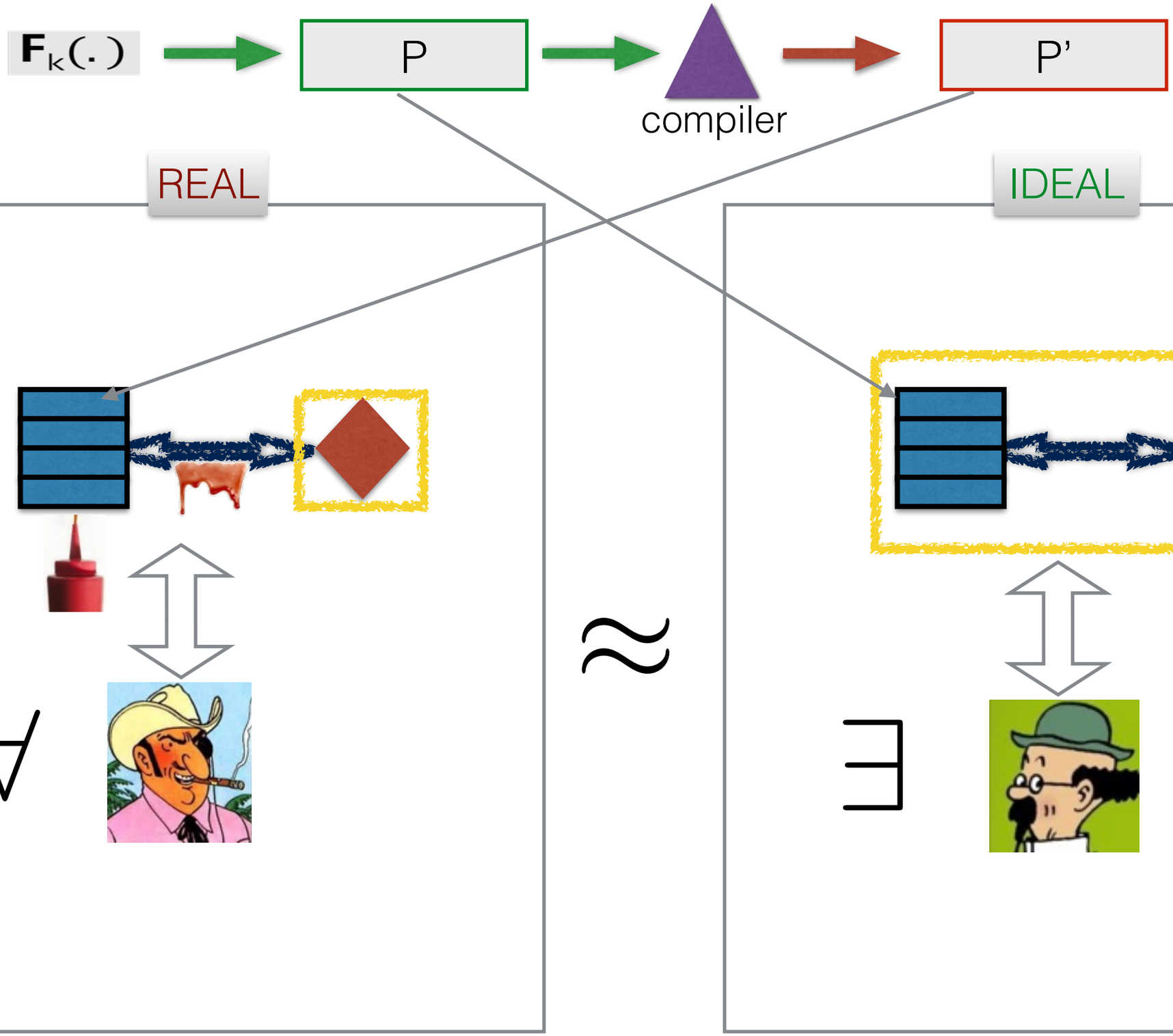
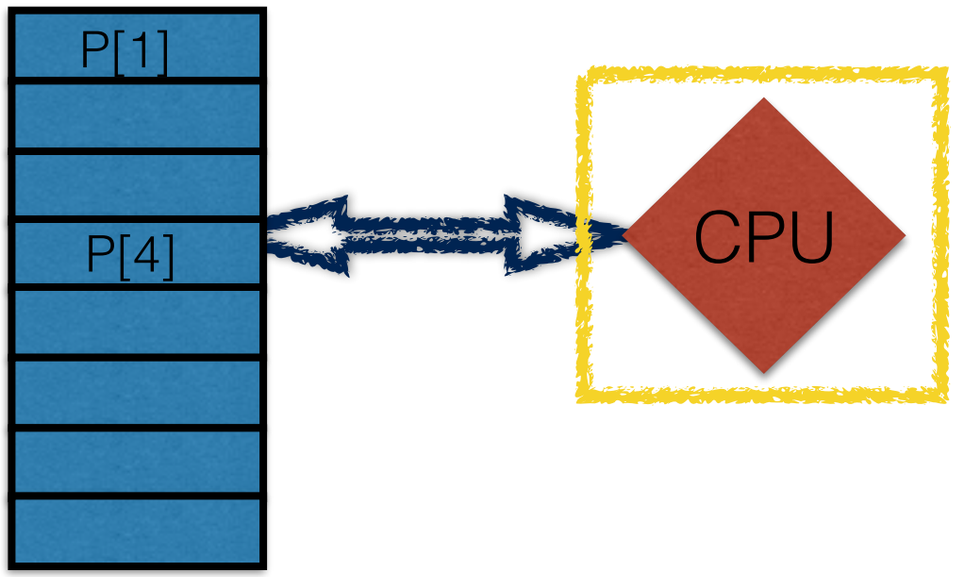


Modular approach: Hybrid world



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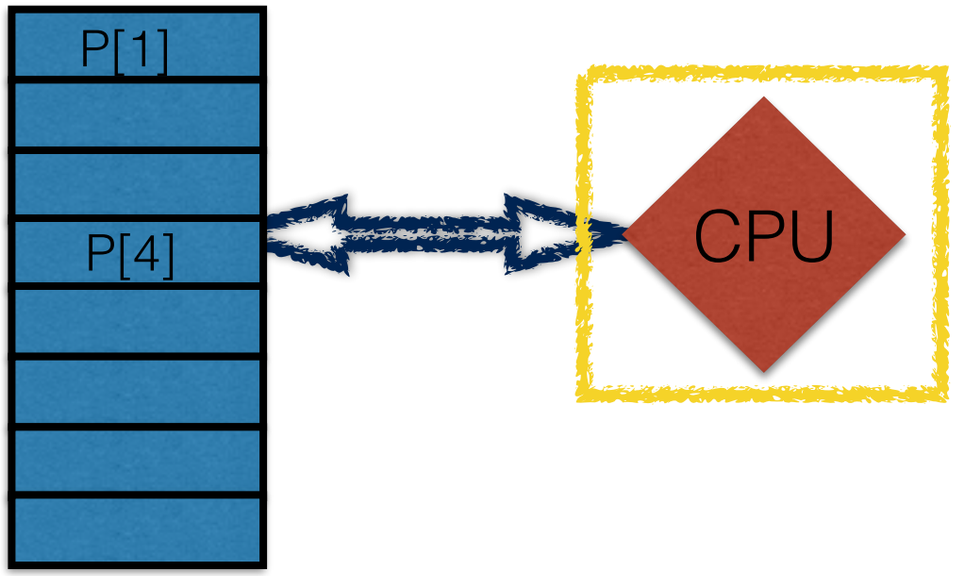

No leakage

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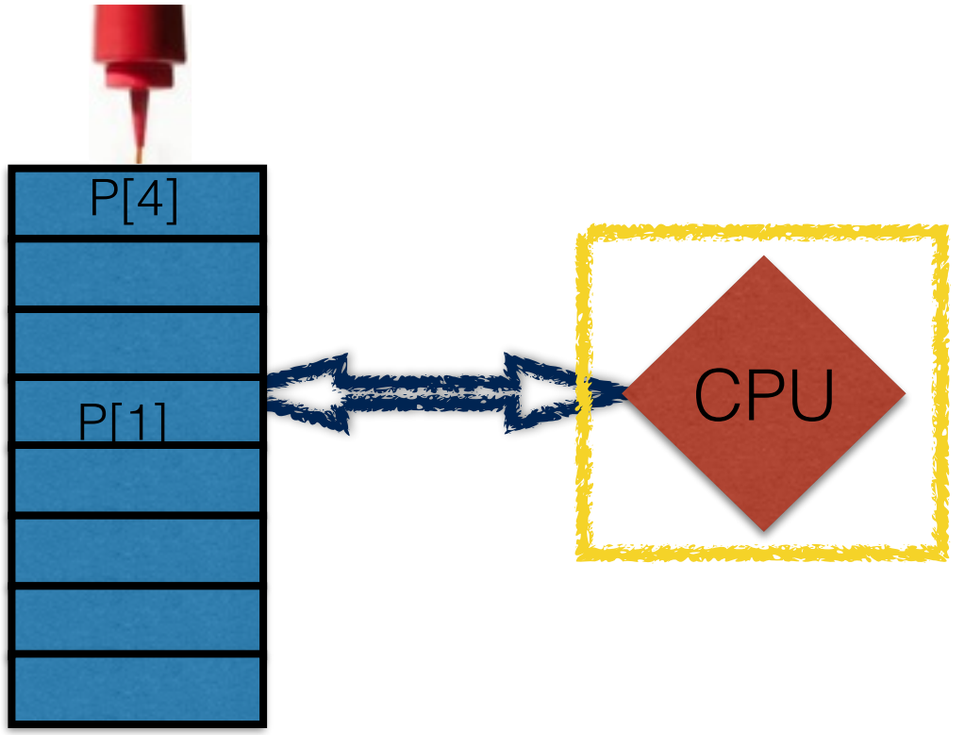

No leakage

Mild tampering:
1. COPY within disk

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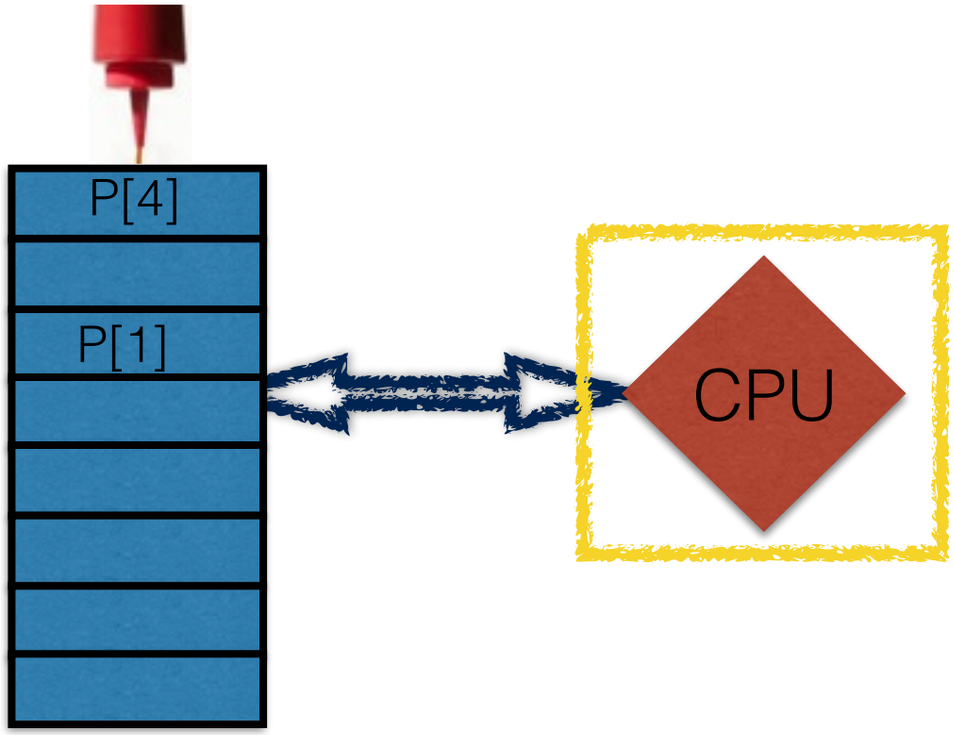

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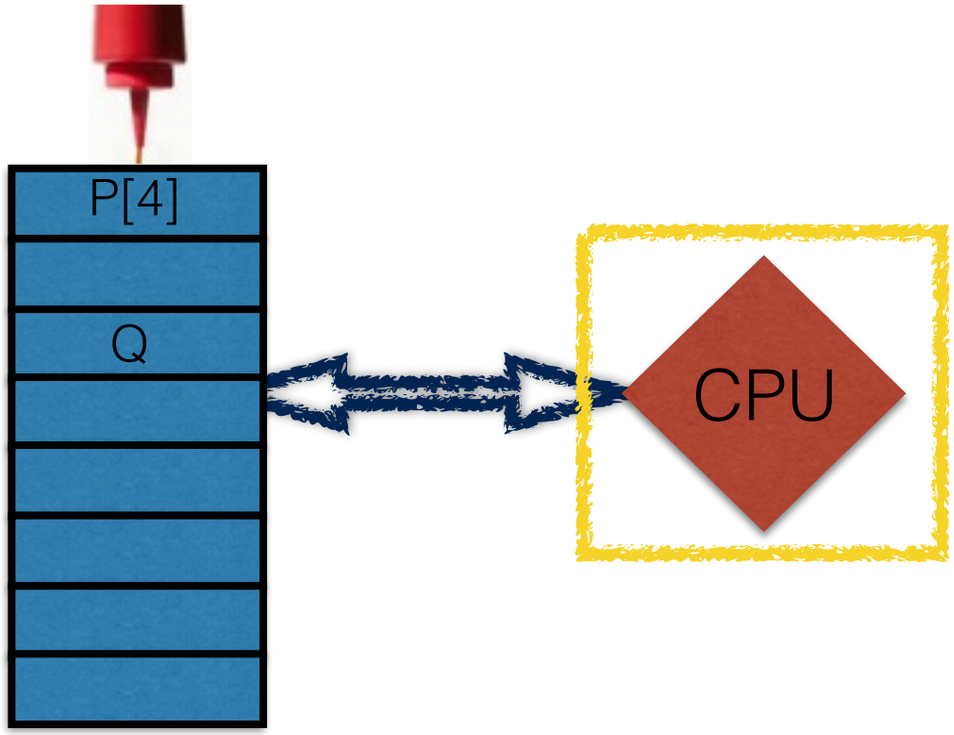

No leakage

Mild tampering:
1. COPY within disk
2. Overwrite

Our construction: Two steps

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P= (P[1],P[2],…)

Step-1

Our construction: Two steps

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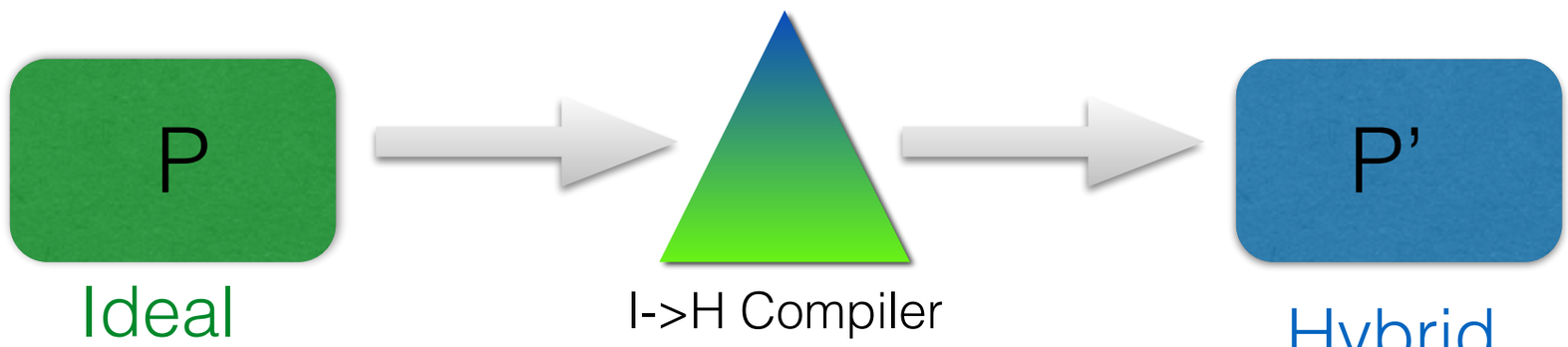
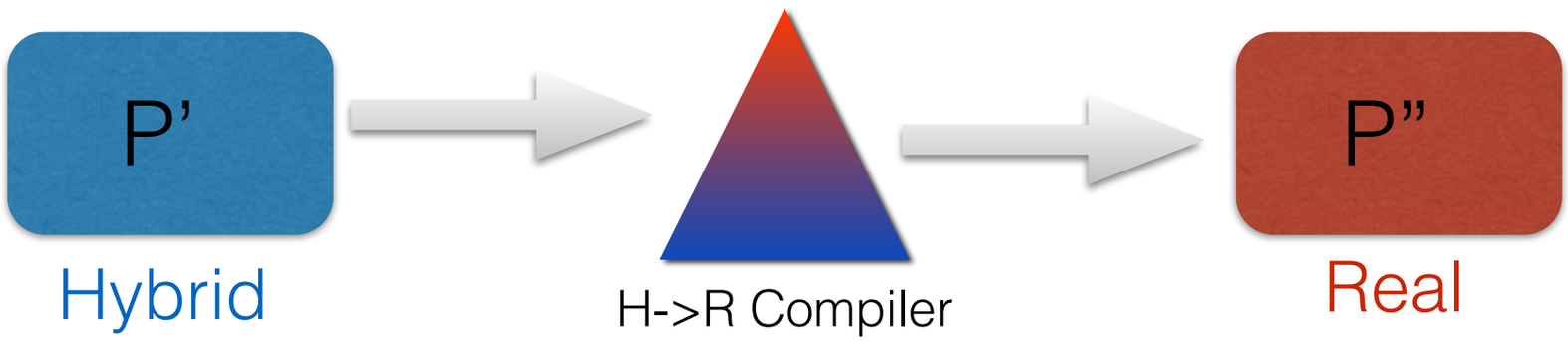


Step-2



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Recall : in hybrid model there is only limited tampering:
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Augment each P[i] by appending:

- A secret level L

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Recall : in hybrid model there is only limited tampering:
1. COPY 2. OVERWRITE

Augment each P[i] by appending:
- A secret level L

- Binds the instructions and secrets
- Guarantees that if the adversary overwrites instructions, it has to overwrite secrets.
  - Otherwise one can just overwrites instructions to output secrets.

Step-1: Ideal to Hybrid compiler

Recall : in hybrid model there is only limited tampering:
1. COPY 2. OVERWRITE

Augment each P[i] by appending:
- A secret level L
- The position i

Protect against copying from one location to another

Step-2: Hybrid to Real compiler

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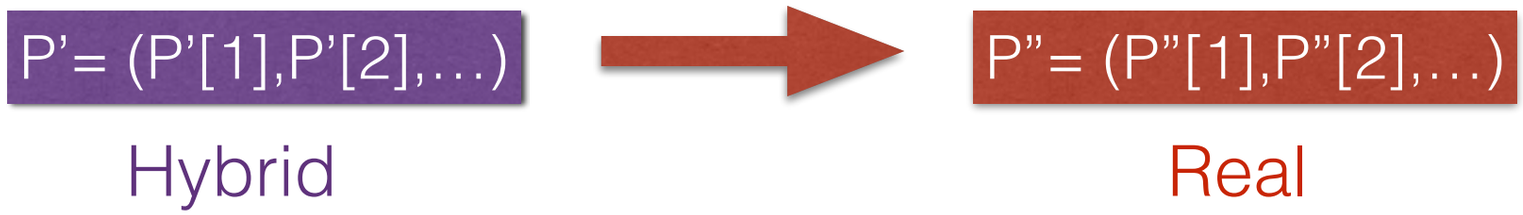

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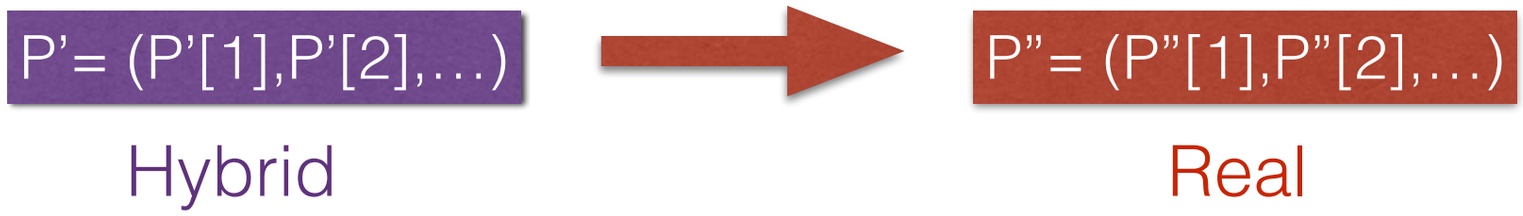

Idea: Encode each P'[i] such that the adversary can only copy or overwrite

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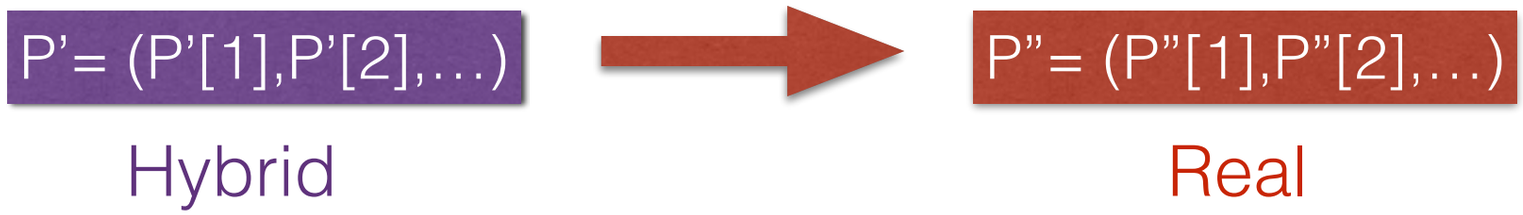

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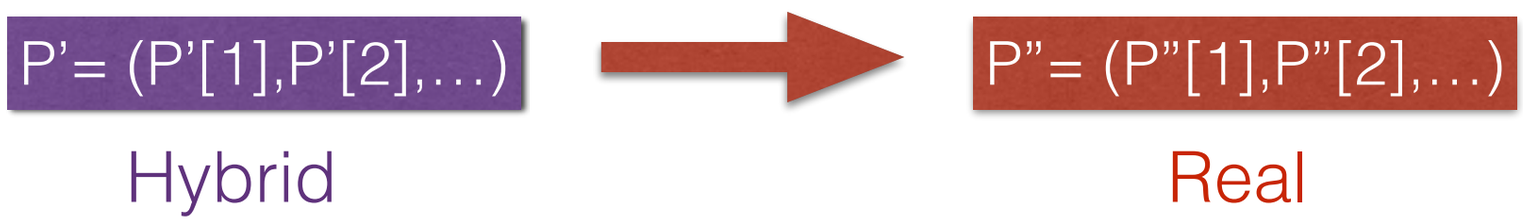
Encode using Non-malleable codes

Step-2: Hybrid to Real compiler



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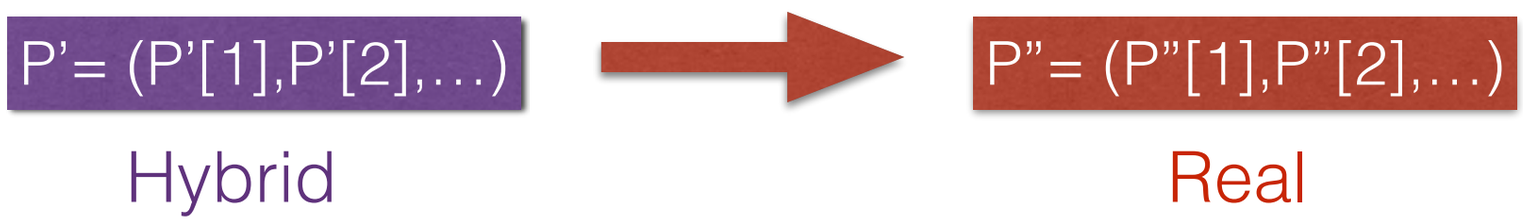

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Non-malleable Codes (DPW10)

An encoding (ENC, DEC) is non-malleable w.r.t. a function family $\mathcal{F}$ if the following holds

$$\forall m, \forall f \in \mathcal{F} \qquad c \leftarrow ENC(m) \qquad c' := f(c) \qquad m' := DEC(c')$$

Then m is equal or unrelated to m'

A suitable instantiation of Non-malleable codes

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- Construction works for split-state $\mathcal{F}$: codeword has two parts which are independently temperable
- Needs Common Random String
- Needs self-destruct

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(P”[i][1],P”[i][2])<—ENC(P’[i])

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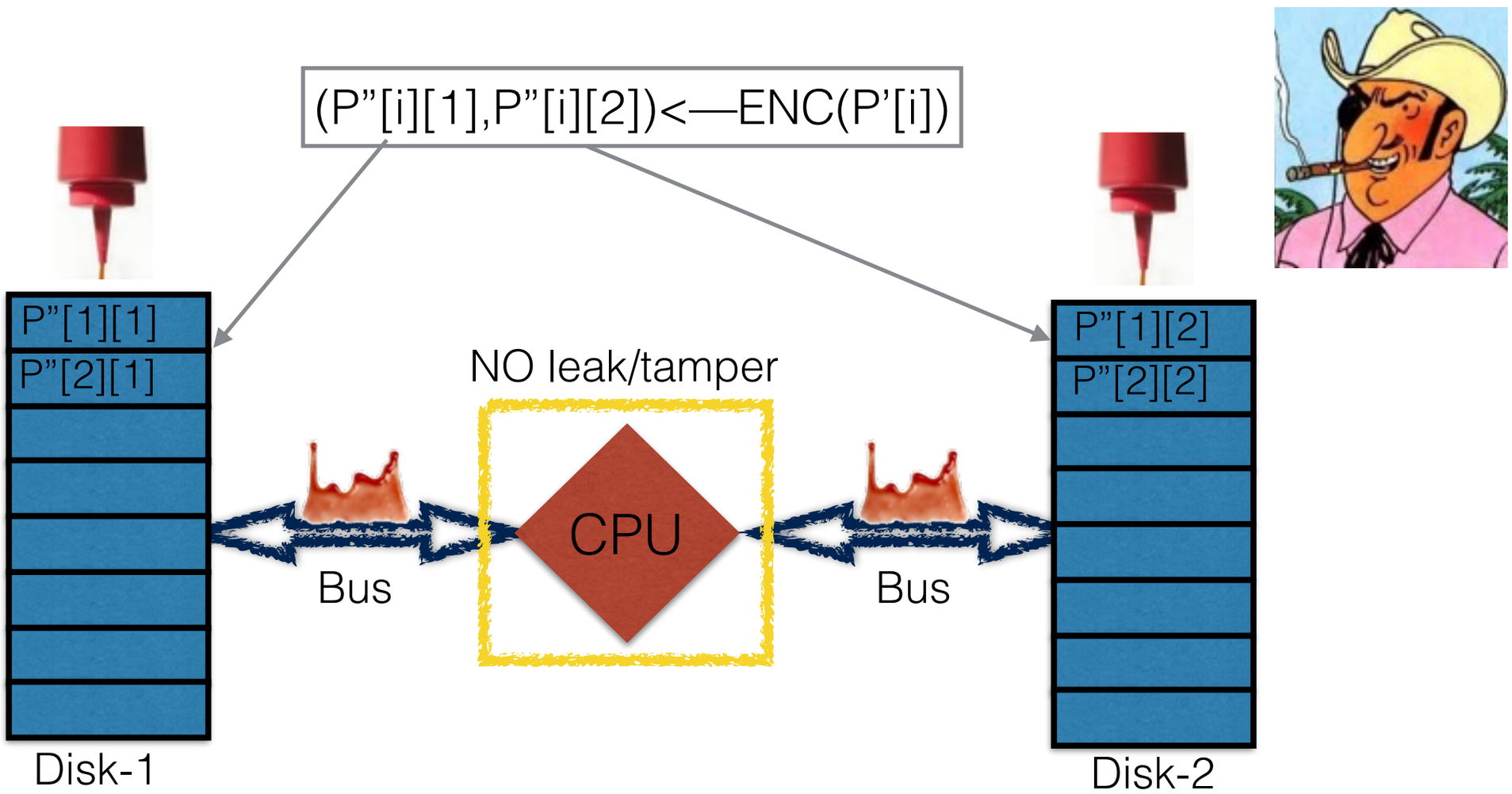

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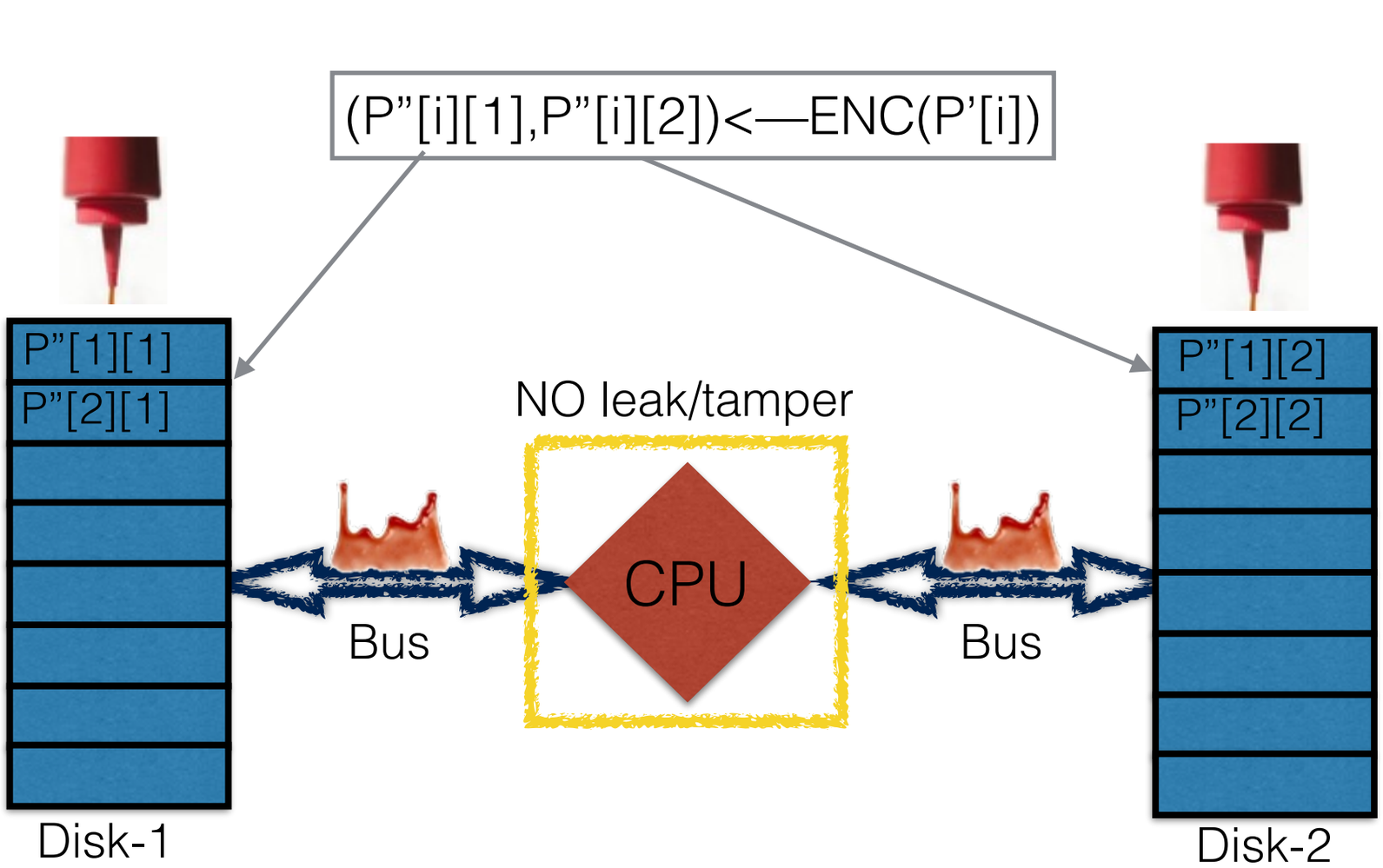
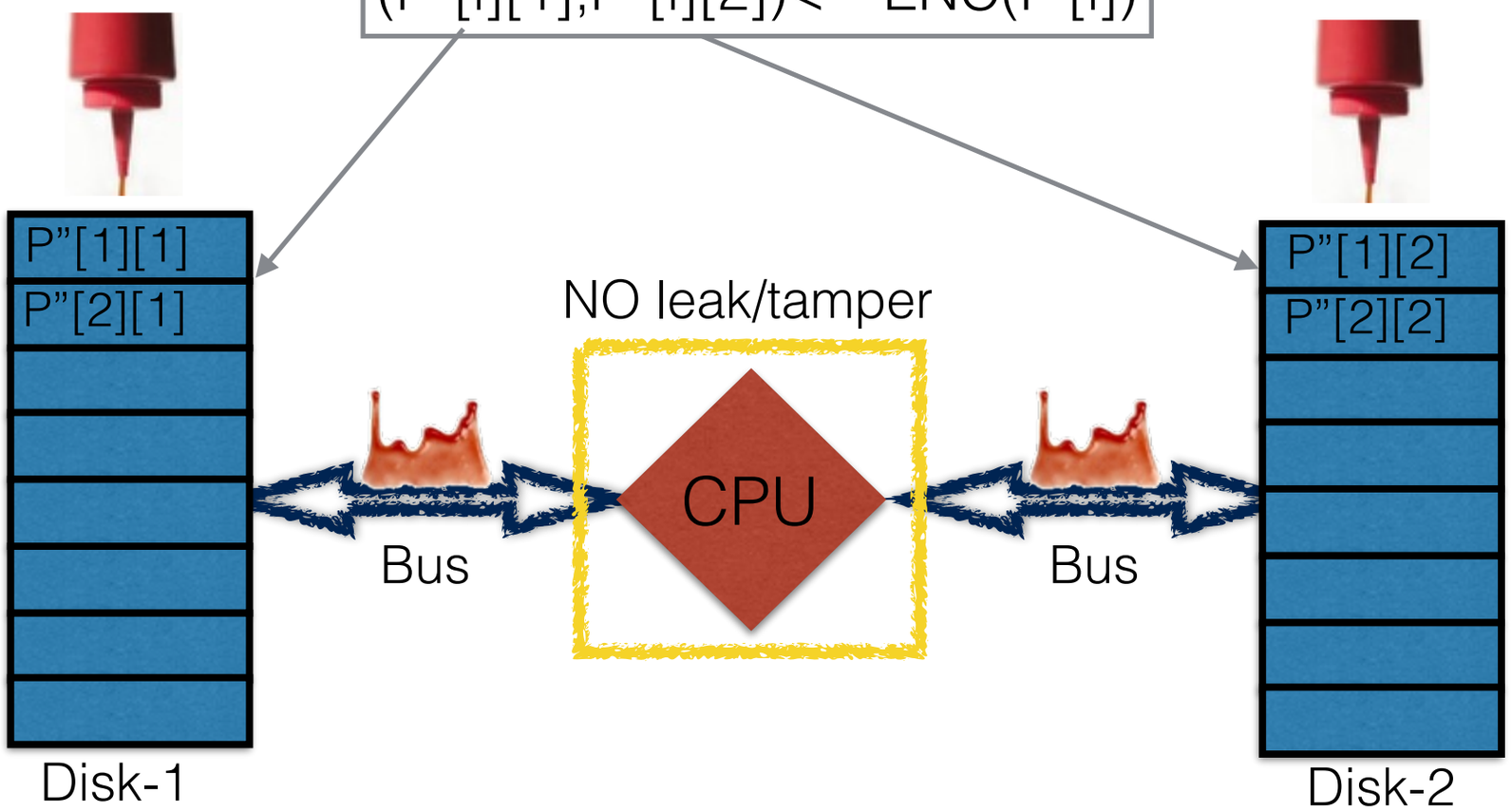


CPU

- CRS is part of description and hardwired.
- stores one untamperable special purpose bit.

Implementing vNA via FMNV14 code



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the self-destruct flag

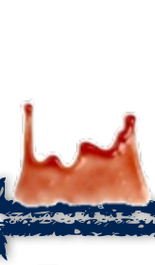
Implementing vNA via FMNV14 code

(P”[i][1],P”[i][2])<—ENC(P’[i])

P”[1][1]
P”[2][1]

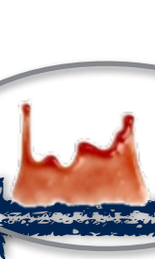
P”[1][2]
P”[2][2]

NO leak/tamper



Bus

CPU



Bus

- P’[i] accessed bounded no. of times.
- CNMC protect against bounded leakage

Disk-1

Disk-2

the self-destruct flag

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- Future direction:

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- Our architecture can withhold significantly stronger tampering: (split-state) than the circuit-oriented approach.
- Since our transformation from Hybrid to Real uses the CNMC in blackbox way, better construction will improve the overall construction.
- Future direction:
  - CPU size depends linearly on sec-param since it has to execute DECODE of CNMC. Can we get constant?

Thank You !